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Multi-threshold transistors cell for low voltage integrated temperature sensing application in digital deep submicron process

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Multi-threshold transistors cell for low voltage integrated temperature sensing application in digital deep submicron process

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ABSTRACT

The rapid shrinking of feature sizes in CMOS processes has enabled high density integration of multi-core systems. However, the corresponding increase in component and local power densities induces thermal stress that can severely affect the reliability of the integrated circuits. To improve the power and thermal management for multi-core systems, an array of temperature sensors is now used to locally monitor the die temperature and provide feedback to the controller for efficient load management and/or load balancing. These temperature sensors must be very small (minimum area overhead) and low power, must have low supply sensitivity, and must provide accurate temperature measurements over a limited operating range.

This thesis provides fundamental analysis of a CMOS Widlar reference generator and the synthesis of a P-Type reverse Widlar temperature sensor. This is followed by the introduction of a 4-transistor multiple threshold voltage (multi-VT) based temperature sensor. Power supply sensitivity analysis and noise analysis are provided for both the 5-transistors reverse Widlar structure and the 4-transistors multi-VT structure. A full design example of a cascoded multi-VT temperature sensor based upon the low-voltage 4-transistor temperature sensor core is also presented. The cascoded structure includes self-bias generators for biasing of the cascode transistors.

The proposed cascode multi-VT temperature sensor based upon the 4-transistor temperature sensor core is implemented in a digital 65nm process with a 1.2V supply voltage. The circuit expresses the threshold voltage directly at the output, does not require a start-up circuit, and provides temperature measurement over an extended operating range. In this

thesis, focus is on how the sensor performs over the -20°C to 100°C temperature range. This sensor can achieve high temperature linearity over this operating range.

In a design example of the cascoded 4-transistor multi-VT sensor implemented in a 65nm process, simulation results were obtained that show a maximum nonlinearity over all process corners of 0.546°C over a 120°C operating range. The supply sensitivity is small with a total variation of 0.44°C due to a ±10% variation in the supply voltage. The combined temperature nonlinearity and temperature error due to supply variations is less than 1°C.

A detailed discussion of the operation of the cascode self-biasing circuits relating to stability, start-up circuits, and equilibrium points is presented. By adapting the contraction mapping principle to the multi-loop self-biased multi-VT temperature sensor, it is shown that the proposed circuit has a single stable equilibrium point and thus does not require a startup circuit.

CHAPTER 1 INTRODUCTION

As multiple-core digital processors, which now are dominant in the high-end processor market, grow in the number of cores per chip, power/thermal management is becoming an increasingly important part of the design process. A critical part of any power/thermal management solution is an array of on-chip temperature sensors that can accurately measure the die temperature at a large number of critical locations on the die. From a practical viewpoint, the total power and area budget for these temperature sensors must be small and self-heating should not compromise the temperature measurements.

The reason for multiple cores stems from the relationship between clock frequency and power usage as they relate to the physics of MOS transistors. At high clock frequencies, the dynamic power dissipation is a significant part of the overall power budget. The dynamic power dissipation associated with standard switching of capacitive loads is characterized by the equation [**1**].

$$P_{dynamic} = \alpha C V_{DD}^2 f \tag{1.1}$$

where α is the activity factor, C is the capacitive load, V_{DD} is the supply voltage, and f is the clock frequency.

From the time of the introduction of the first microprocessor, the Intel 4004, in late 1971 up until the early 2000's, the trend in digital processors was ever-increasing clock frequencies. Clock frequencies continued to climb from the 740KHz of the Intel 4004 up to the Gigahertz range of the Intel Pentium class processors in the early 2000's. But a peak in clock frequency was reached at around the 3.0GHz range. At these peak frequencies, power consumption in the digital processors was so large that further increases in frequency would

introduce cooling challenges with no known practical solution. Thus, multiple cores were introduced to increase productivity in digital processors without increasing clock speed. Instead of increasing the speeds of one single core, many cores were implemented on a single chip to perform multiple tasks in parallel when needed. This continued the trend in productivity and computation that has been going on for decades. To continue this trend into the future, computer processor manufacturers and other digital processor designers have revealed that more cores will be added to each new generation of chips. According to the International Technology Roadmap for Semiconductors (ITRS), the number of cores per chip will continue to increase through 2024 exponentially resulting in over 100 cores per chip by the end of that span, as shown in Figure 1-1 [**2**]. As the number of cores increase, so does performance, but at a cost of more power consumed.

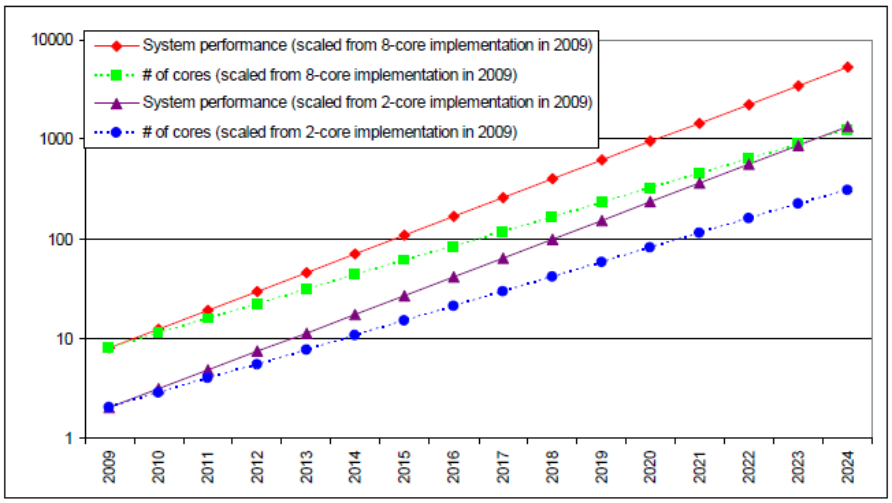


Figure 1-1: SOC consumer stationary performance trends[1] (ITRS Update 2010). [2]

Intel is scheduled to release 8-core and 10-core chips in the near term [**3**]. On the other hand, the graphics processing industry already uses over a thousand cores in some of their high-end chips. The graphics giant nVidia uses 1024 cores (dual 512 core) in its latest

1. Plot based on homogeneous 2-core architecture template and heterogeneous 8-core architecture template. System performance metric is the normalized product of number of cores and corresponding core frequency [**2**].

Graphics Processing Unit (GPU), the GeForce GTX590, to create the smoothest visual experience for computer users whether playing graphics-intensive games or running applications on multiple displays simultaneously [**4**]. As power consumed per chip increases with the number of cores per chip, a need for better power management exists. Current power management methods include sensing temperature and voltages to vary fan speeds or decrease clock frequencies when devices become too hot. Ideally, in a multi-core system, the health of each core should be managed and if existing methods of power management are extended to multi-core systems, temperature and/or voltage sensing at one or more sites on each core would be necessary. This can be done today with a rather small number of sensors since there are relatively few cores per chip but in the future with projections of over 100 cores on a single die, the number of sensors needed for power management will become very large. Thus, there is a critical need for on-chip temperature sensors in sub-micron digital processes which are accurate, small, low power, and process insensitive.

As the power requirements of computer processors continue to increase with each new generation of chip, they will dissipate more heat and must be more aggressively cooled to maintain acceptable lifetimes. According to the graph below from the ITRS 2010 Update, total power consumption in semiconductor devices with high performance processing capabilities is currently around 125W. By 2016, the amount of power consumed per chip is projected to surpass 200W and eventually approach 500W by 2024 if current trends in power requirements continue [**2**]. The resultant heat generated must be dissipated and taken off chip to avoid damaging or destroying the device.

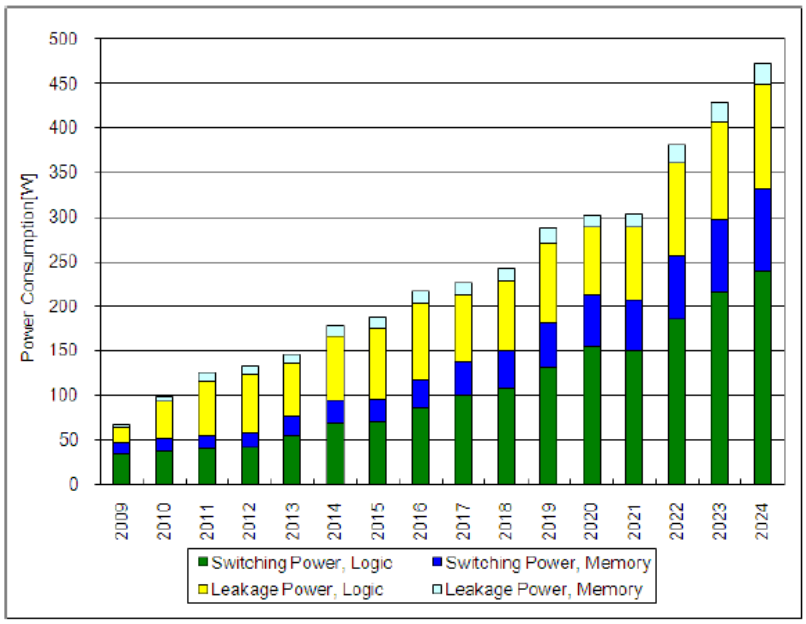


Figure 1-2: SOC consumer stationary power consumption trends (ITRS Update 2010) [2]

In general, temperature sensors in chips today are crude and not very accurate [**5**] [**6**]. With inaccurate temperature sensors, on-chip power management systems cannot optimally manage performance to avoid stress-induced damage such as electromigration. If temperature sensors could be made small enough with sufficiently low power requirements while retaining accuracy to the 1^{o}C level, multiple sensors could be placed at critical locations on each core and in the critical paths where heating causes excessive stress and wear on the integrated circuit. With this real-time temperature information, power management algorithms can be developed that will maximum performance of the integrated circuit while still maintaining target reliability and lifetime metrics. With better temperature sensors and with the temperature information integrated into the power management unit (PMU), cores can be better utilized, spreading the load to many cores without overheating any particular core or any critical sublocks within a core or between cores.

In a paper published by Black in 1969 [**7**], the relationship between temperature, electrical stress, and median-time-to-failure (MTF) associated with electromigration in aluminum interconnects was discussed. Black described the process of electromigration and presented a model of this effect in which temperature is exponentially related to the decrease in MTF. It follows from this exponential relationship that small increases in temperature result in dramatic decreases in the MTF and that if operated above some critical temperature, the MTF will be unacceptably short. Thus, if sensors can accurately tell when a critical threshold temperature is met, electromigration failure can be probabilistically reduced to an acceptable level or, equivalently, the MTF of a processor can meet a predetermined target value. There are many different ways the system can be architected to meet target MTF goals if accurate temperature information across a die is available. Conceptually, one strategy could include temporarily disabling any particular core when the temperature at sensors in that core becomes too high. Another strategy could be dynamically adjusting clock frequencies or supply voltages to bound temperature throughout a core or throughout a die, and yet another could be to dynamically assign tasks between cores based upon where heating is problematic. In this thesis, focus will be restricted to the temperature sensors themselves, which will provide enabling technology for those designers that have responsibility for the PMU or the system architectures.

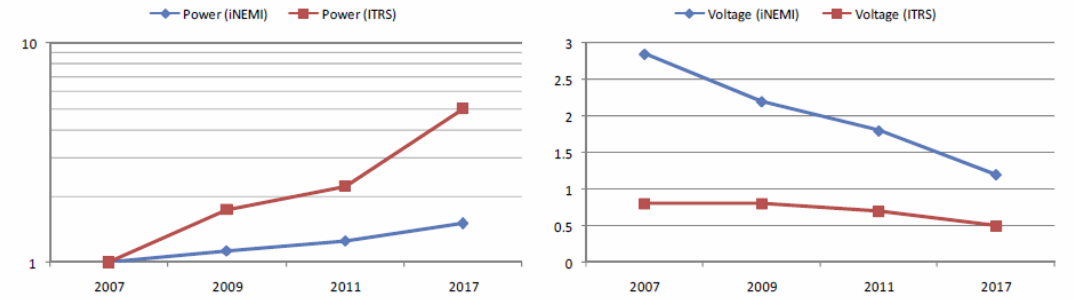


Figure 1-3: ITRS-iNEMI System-to-Chip Power Comparison Trends (ITRS) [2]

Another trend in digital processes is the reduction in supply voltage. As digital voltage supply levels continue to decline over time, designs for multi-core temperature sensors must also work at these low supply voltages. This means designs created today must be relatively insensitive to supply voltage when characterizing their performance. By 2017, ITRS predicts supply voltages in digital processes will decline to below the 1V level [**2**]. This leaves little headroom in analog circuits created in these digital processes. As such, temperature sensors that scale with technology must also be able to operate at low supply voltages. This work will include considerations for operating temperature sensors at low supply voltages.

1.1 THESIS OUTLINE

The research results presented in this thesis primarily focus on temperature sensor design. In particular, a new temperature sensor circuit structure – the multi-VT 4-transistors cell and its cascoded version is presented. A brief outline of each chapter follows.

An analysis of the conventional CMOS Widlar and reverse Widlar reference generator, as well as the analysis and synthesis of the 5-transistors temperature sensor derived from the reference generator structure is presented in Chapter 2. Power supply sensitivity analysis and noise analysis are presented as appendixes.

The new multi-VT based temperature sensor is introduced in Chapter 3. The DC transfer characteristics are presented to illustrate the operating points of the circuit with different threshold voltages. The operation of the circuit is analyzed and a design example

for high temperature sensing applications is shown. Power supply sensitivity analysis and noise analysis are included in appendixes.

The design of a fully-cascoded multi-VT temperature sensor operating over the temperature range from -20°C to 100°C is presented in Chapter 4. Extensive simulation results, including the noise performance, are discussed. A cascode self-bias DC loop test based on the contraction mapping principle is discussed. This loop test is used to determine the stable equilibrium operating point(s) of the circuit.

Conclusions from the work done presented in this thesis and directions on future research on the multi-VT structure comprise Chapter 5.

CHAPTER 2 ANALYSIS OF CMOS REFERENCE GENERATOR AND SYNTHESIS OF REVERSE WIDLAR TEMPERATURE SENSOR

2.1 INTRODUCTION

Voltage references, bias generators, current references, current sources, and temperature sensors are all key building blocks that find widespread applications throughout the semiconductor industry. Although the intended uses of these building blocks appear to be diverse, the circuit structures that are used to build these functional blocks are very similar and often identical. More specifically, it is often the case that a specific circuit used in one application serves as a bias generator, in another application it serves as a voltage reference, in another application as a current source, and in yet another application as a temperature sensor. But although the circuit structure may be the same, the operating points and the device sizing may be different from one application to another.

2.2 CMOS REFERENCE GENERATOR

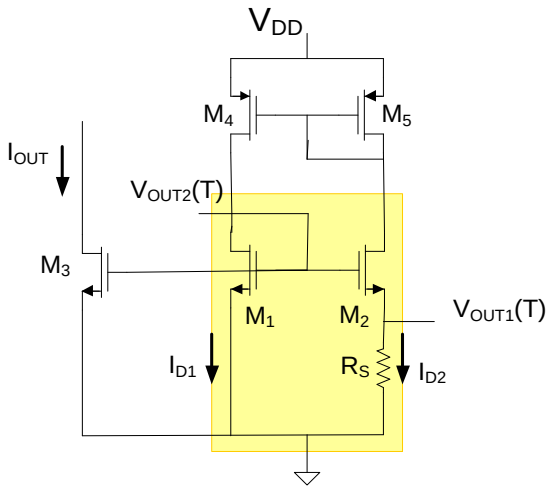


Figure 2-1: Generator circuit based upon Widlar Current Mirror

One example of such a circuit is shown in Figure 2-1. One way to view this circuit is to observe that the components in yellow form a Widlar Current Mirror and transistors M_4 and M_5 form a basic current mirror. These current mirrors are cross-coupled with the output of each mirror driving the input of the other mirror. This can thus be viewed as a two-mirror feedback loop. Voltages V_{OUT1} and V_{OUT2} can be used as biasing voltages and when used as such, it becomes a bias voltage generator. By mirroring the currents from M_1 and M_2 through M_3, a current source or current reference is obtained.

The square-law model is often used to model the strong-inversion operation of the MOS transistor [**8**]. In this model, the gate current is assumed to be 0 and the drain current is given by the expression

$$I_D = \begin{cases} 0 & \textit{Cutoff} \\ \mu C_{ox} \dfrac{W}{L}\left(V_{GS} - V_{TH} - \dfrac{V_{DS}}{2}\right)V_{DS} & \textit{Triode} \\ \mu C_{ox} \dfrac{W}{2L}\left(V_{GS} - V_{TH}\right)^2\left(1+\lambda V_{DS}\right) & \textit{Saturation} \end{cases} \tag{2.1}$$

where

$$V_{TH} = V_{TH0} + \gamma\left(\sqrt{\phi - V_{BS}} - \sqrt{\phi}\right)$$

In these model equations, W and L denote the width and length of the channel of the MOS transistor, the parameters {μ, C_{OX}, V_{TH0}, γ, and ϕ} are model parameters, and the subscripted voltages are port voltages of the device. This same equation applies for both n-channel and p-channel devices but when distinction is necessary, a subscript n or p will be added.

A straightforward analysis of the circuit structure of Fig. 2.1 based upon the standard square-law model of the MOS transistors follows. In this analysis, it will be assumed that all transistors are operating in the strong-inversion saturation region.

The current mirror comprised of M_4 and M_5 has a mirror gain M characterized by the equation

$$I_{D1} = MI_{D2} \tag{2.2}$$

where

$$M = \frac{W_4/L_4}{W_5/L_5} \tag{2.3}$$

Define K by the expression

$$\frac{W_2}{L_2} = K\frac{W_1}{L_1} \tag{2.4}$$

It follows from Kirchhoff's Voltage Law (KVL) that

$$V_{GS1} = V_{GS2} + V_{OUT1} \tag{2.5}$$

Ignoring the output conductance (λ) and the body effect (γ) in the square-law device model, this expression can be rewritten as

$$\sqrt{\frac{2I_{D1}}{\mu_n C_{ox}\left(W_1/L_1\right)}} + V_{TH1} = \sqrt{\frac{2I_{D2}}{\mu_n C_{ox}\left(W_2/L_2\right)}} + V_{TH2} + I_{D2}R_S \tag{2.6}$$

Substituting (2.1) and (2.4) into (2.6) and assuming $V_{TH1}=V_{TH2}$ yields

$$\sqrt{\frac{2I_{D2}}{\mu_n C_{ox}\left(W_1/L_1\right)}}\left(\sqrt{M}-\frac{1}{\sqrt{K}}\right)=I_{D2}R_S \tag{2.7}$$

Hence

$$I_{D2}=\frac{2}{\mu_n C_{ox}\left(W_1/L_1\right)}\cdot\frac{1}{R_S^2}\left(\sqrt{M}-\frac{1}{\sqrt{K}}\right)^2 \tag{2.8}$$

$$I_{D1}=\frac{2}{\mu_n C_{ox}\left(W_1/L_1\right)}\cdot\frac{M}{R_S^2}\left(\sqrt{M}-\frac{1}{\sqrt{K}}\right)^2 \tag{2.9}$$

And in terms of V_{OUT1}

$$V_{OUT1}=\frac{2}{\mu_n C_{ox}\left(W_1/L_1\right)}\cdot\frac{1}{R_S}\left(\sqrt{M}-\frac{1}{\sqrt{K}}\right)^2 \tag{2.10}$$

$$V_{OUT2}=V_{TH1}+\frac{2}{\mu_n C_{ox}\left(W_1/L_1\right)}\cdot\frac{\sqrt{M}}{R_S}\left(\sqrt{M}-\frac{1}{\sqrt{K}}\right) \tag{2.11}$$

Assuming that all transistors are in saturation, it can be observed from the expressions above that the voltages V_{OUT1} and V_{OUT2}, as well as the currents I_{D1} and I_{D2} are independent of V_{DD}. By taking the node voltage output from either V_{OUT1} or V_{OUT2}, the circuit serves as a voltage reference; whereas by mirroring the current from M_1 and M_2, the circuit serves as a current source or current reference.

In this circuit, there are 3 parameters that are temperature dependent, the carrier mobility μ, the threshold voltage V_{TH0}, and the resistor R_S. The circuit can be designed through clever manipulation of the design variables {W_1/L_1, W_2/L_2, W_3/L_3, W_4/L_4, W_5/L_5,

and R_S}, so that the output voltages and/or currents are either sensitive to or relatively insensitive to temperature. If the circuit is designed so that the outputs are substantially temperature dependent with a monotone relationship between the output and temperature, the circuit can serve as a temperature sensor.

Although any circuit that provides a monotone relationship between output and temperature could be used as a temperature sensor, some relationships are much more useful than others. From a practical viewpoint, a good temperature sensor will generally have a rather large change in the output with temperature and it is generally considered preferable to have this relationship be linear. Other desirable properties of a temperature sensor include low sensitivity to process variations, relaxed matching requirements, a minimum number of trims, low power dissipation, small area, and often a wide temperature operating range.

Due to the multiple possible purposes that this circuit can serve, it shall be simply termed as a "Generator" circuit. One interesting property of this and other variations of generator circuits is that there is no electrical "input" to the circuit beyond the supply voltage V_{DD} and the outputs of interest in the generator circuit are quite independent of V_{DD}. One key requirement of many generator circuits is that the outputs be quite insensitive to V_{DD}.

Variants of the basic two-mirror feedback loop of Figure 2-1 are shown in Figure 2-2 where in the preferred mode of operation of these circuits, all devices are operating in the saturation region.

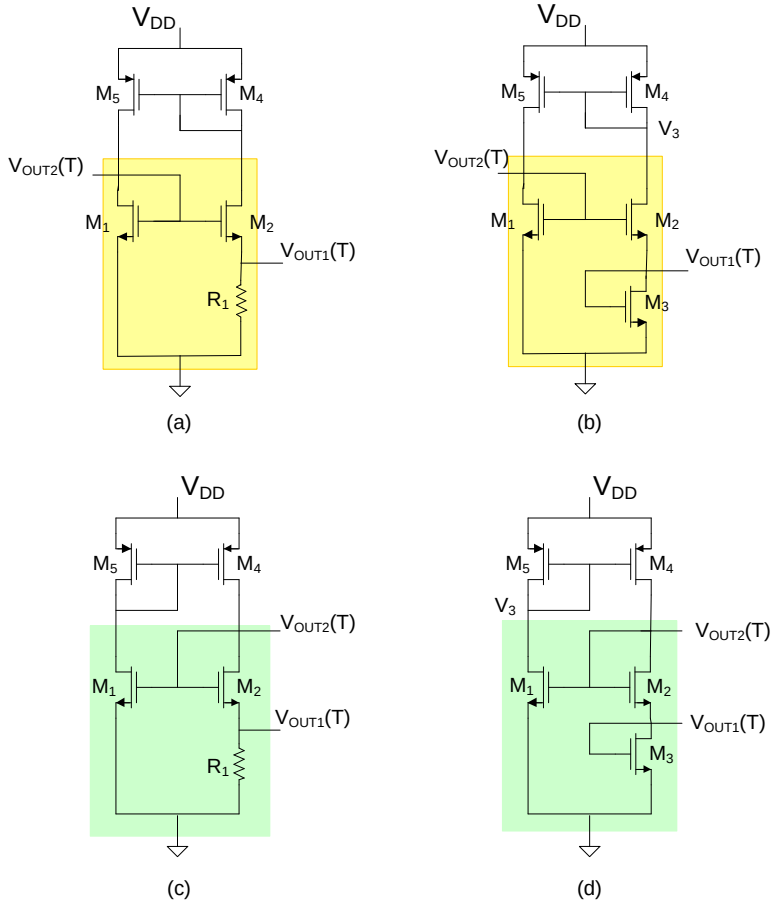


Figure 2-2: VDD-independent Bias Generators a) Widlar, b) Widlar with diode connected transistor, c) Reverse Widlar, d) Reverse Widlar with diode connected transistor (start-up circuits not shown)

The circuits in Figure 2-2(a) and Figure 2-2(b) are most widely used as bias voltage and current generators [**9**] [**10**] [**11**] [**12**] [**13**] [**14**] and in these circuits, the subcircuit shown in yellow is the Widlar current mirror configuration. The two circuits on the right of this figure can be derived from the circuits on the left by replacing the resistor R_1 with a corresponding diode-connected transistor, M_3. The circuits in Figure 2-2(c) and Figure 2-2(d) have received some attention for use as references [**15**] and, in particular, have been used as temperature sensors [**16**]. The subcircuit shown in green in these structures is sometimes termed the reverse-Widlar current mirror configuration. All of these circuits have the property that the currents flowing in the devices and the labeled internal node voltages are nearly independent

of V_{DD} and the weak V_{DD} dependence is primarily due to the finite output impedance of the transistors. Since the labeled node voltages are nearly independent of V_{DD}, these circuits can be viewed as V_{DD}-independent voltage generators or current generators.

2.3 THRESHOLD EXTRACTION CIRCUIT

The resistorless version of the Widlar/Reverse-Widlar reference generator circuits in Figure 2-2(b) and (d) can directly express the MOS threshold voltage at the output node voltages V_{OUT1} and V_{OUT2}. As a review of previous work published in [**17**] [**18**], the reverse-Widlar based threshold extraction circuit analysis is presented here.

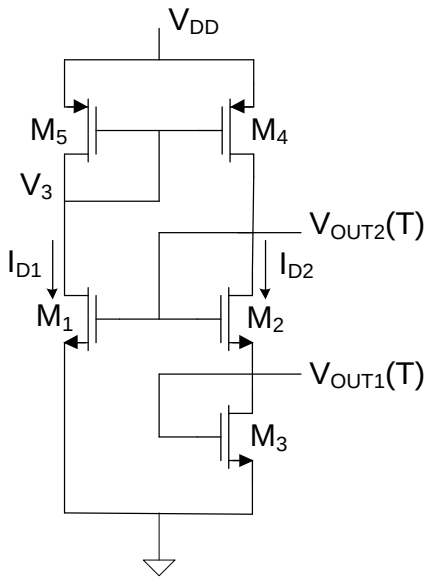


Figure 2-3: Reverse-Widlar Threshold Extraction Circuit

Based on the notations shown in Figure 2-3, assuming an ideal square-law model and neglecting output conductance effects, the following equations are written to describe the operation of the circuit:

$$I_1 = \frac{\mu_n C_{ox}}{2}\frac{W_1}{L_1}(V_{OUT2} - V_{Tn1})^2 \tag{2.12}$$

$$I_2 = \frac{\mu_n C_{ox}}{2}\frac{W_2}{L_2}(V_{OUT2} - V_{OUT1} - V_{Tn2})^2 \tag{2.13}$$

$$I_2 = \frac{\mu_n C_{ox}}{2}\frac{W_3}{L_3}(V_{OUT1} - V_{Tn3})^2 \tag{2.14}$$

$$I_{D2} = MI_{D1} \tag{2.15}$$

Equations (2.12) – (2.15) are then solved to express the output node voltages.

$$V_{OUT1} = \frac{(V_{Tn1} - V_{Tn2})\sqrt{\frac{W_2/L_2}{W_3/L_3}} + V_{Tn3}\left(1 - \sqrt{\frac{W_2/L_2}{M(W_3/L_3)}}\right)}{1 + \sqrt{\frac{W_2/L_2}{W_3/L_3}} - \sqrt{\frac{W_2/L_2}{M(W_1/L_1)}}} \tag{2.16}$$

$$V_{OUT2} = \frac{V_{Tn1}\left(1 + \sqrt{\frac{W_2/L_2}{W_3/L_3}}\right) - V_{Tn2}\sqrt{\frac{W_2/L_2}{M(W_1/L_1)}} - V_{Tn3}\sqrt{\frac{W_2/L_2}{M(W_1/L_1)}}}{1 + \sqrt{\frac{W_2/L_2}{W_3/L_3}} - \sqrt{\frac{W_2/L_2}{M(W_1/L_1)}}} \tag{2.17}$$

In a standard CMOS process, the threshold voltages are assumed to be approximately equal to each other. Hence, assuming that all NMOS transistors M_1, M_2 and M_3 have the same threshold voltages, (2.16) and (2.17) can be simplified to be

$$V_{OUT1} = V_{Tn}\frac{1 - \sqrt{\frac{W_2/L_2}{M(W_3/L_3)}}}{1 + \sqrt{\frac{W_2/L_2}{W_3/L_3}} - \sqrt{\frac{W_2/L_2}{M(W_1/L_1)}}} \tag{2.18}$$

$$V_{OUT2} = V_{Tn} \frac{1+\sqrt{\frac{W_2/L_2}{W_3/L_3}} - 2\sqrt{\frac{W_2/L_2}{M(W_1/L_1)}}}{1+\sqrt{\frac{W_2/L_2}{W_3/L_3}} - \sqrt{\frac{W_2/L_2}{M(W_1/L_1)}}} \tag{2.19}$$

From (2.18) and (2.19), it is shown that the output node voltages directly express the MOS threshold voltage where the linear coefficients are given by the transistors W/L ratios and the current mirror gain M which is also a ratio of W/L values.

In the widely used BSIM4 model, the threshold voltage temperature dependence model is given by [**19**].

$$V_{TH}(T) = V_{TH}(TNOM) + \left(KT1 + \frac{KT1L}{L_{eff}} + KT2 \cdot V_{bseff} \right) \cdot \left(\frac{T}{TNOM} - 1 \right) \tag{2.20}$$

where T is temperature in K, TNOM is set at 300K; KT1, KT1L, and KT2 are process dependent constant; L_{eff} is the effective length of the transistor which is approximately equal to the length L, and V_{bseff} is the effective bulk to source voltage. If V_{bseff} is temperature independent, this model predicts a linear dependence of the threshold voltage with temperature. Hence, provided that the MOS threshold voltage temperature dependence model is close to being accurate, the output node voltages of the reverse-Widlar threshold extraction circuit are nearly linear with temperature. This linear relationship between output and temperature is one of the most desirable characteristics of a temperature sensor.

While the analytical results show good temperature linearity, it is inevitable that the output node voltages will show some temperature nonlinearity due, in part, to neglecting the output conductance effects in the previous analysis and due to higher-order temperature

effects that are not included in the temperature dependent threshold voltage model of (2.19). The effect of finite output conductance on the circuit of Fig. 2-3 has been investigated in [**18**] where it was shown that there is no closed-form explicit analytical expression for the temperature dependence of the output voltage if the output conductance (λ parameter) is included in the square-law analytical model. However, the authors in [**18**] did provide some analytical insight on compensating for the higher-order temperature dependence, and also provided numerical iterative device sizing strategies to achieve good temperature linearity with nonlinear errors of well under 1°C over a temperature range from -20°C to 100°C.

In addition, the application note in [**20**] suggests that the first-order threshold voltage temperature coefficient is not a constant value and that it is given by

$$\frac{\delta V_{THn}}{\delta T} = \frac{\Phi_{ms}}{T} + 2\frac{\Phi_F}{T} + t_{ox}\frac{\sqrt{\epsilon_s q N_a}}{\epsilon_{ox}\sqrt{\Phi_F}}\cdot\frac{\delta\Phi_F}{\delta T} - 6\frac{K}{q} - 2\frac{E_{g0}}{qT} \tag{2.21}$$

where Φ_{MS} is metal-semiconductor difference work function, Φ_F is the Fermi potential, ε_{ox} is the oxide permittivity ($34.5\text{x}10^{-12}$ F/m), t_{ox} is the oxide thickness, ε_S is the silicon permittivity ($105.4\text{x}10^{-12}$ F/m), K is the Boltzmann constant ($1.38\text{x}10^{-23}$ J/K), q is the electron charge, and Eg0 is the extrapolated value of the band-gap at 0K (1.21eV). Although (2.21) shows that the MOS threshold voltage is not perfectly linear with temperature, simulated and measurement results provided in [**20**] show that the threshold voltage temperature coefficient does not vary significantly across a 150K temperature range. This suggests that the threshold voltage can be approximated as being nearly linear with temperature. Hence, good temperature linearity can be expected from various threshold voltage extraction circuits

through clever circuit design and compensation. But compensation for the modest nonlinearity can improve performance of the temperature sensor [**17**] [**18**].

2.4 STARTUP ISSUE

All of the threshold extraction circuits of Figure 2-2 along with several other CMOS reference generator circuits are known to have multiple stable operating points. One of these operating points is the desired operating point and when operating at this point, the circuit provides the desired performance. The other operating points are considered to be undesirable operating points and the performance of the circuit when operating at any of the other operating points is not desirable. Any circuit that has more than one stable operating point can get stuck at an undesirable operating point. Various explanations are given in [**12**] [**21**] [**8**] about the undesirable operation of such circuits but they do not clearly or rigorously illustrate the existence of multiple operating points. Unfortunately, a direct DC simulation or transient simulation from any circuit simulator may or may not detect all of the stable operating points because circuit simulators are designed to provide or converge to a single solution.

Any circuit that has stable operating points can be guaranteed to operate at a desired operating point only if the circuit is modified in such a way that the undesired stable operating points are eliminated. The modification of reference generators that is made to eliminate the undesired operating points is generally referred to as the addition of a “start-up” circuit. This terminology may be somewhat misleading since the implication is that the “start-up” circuit forces the circuit to avoid the undesired operating points. Actually, the “start-up” circuit is a circuit modification that removes the undesired operating points so that

the circuit only has a single stable operating point. With a single stable operating point, the concern about getting stuck at an undesired operating point has been eliminated since the undesired operating point has been eliminated.

Hence, it is important to have a rigorous method to determine the possible operating points of a circuit, and provide insight into both the need for and the effectiveness of a startup circuit that is used to eliminate the undesired operating points.

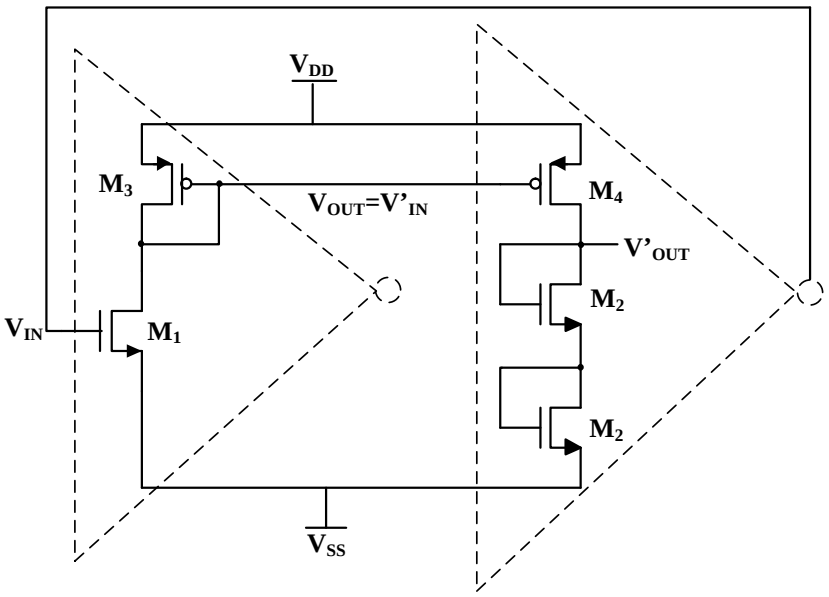


Figure 2-4: Cascade of n-channel/p-channel input inverters with source degradation transistor

As shown in Figure 2-4, the CMOS reference generator circuit of Figure 2-3 can be viewed as two cascaded inverters in a loop, where V_{IN} is connected to V'_{OUT}. The general transfer characteristics of an inverter can be depicted as shown in Figure 2-5. The transfer curve generally has a low-gain region for low and high inputs and a higher-gain region in the middle. Since the gain is negative (inverting), the slope is always negative and, depending on how the devices are sized, the magnitude of the slope can be made larger or smaller than 1.

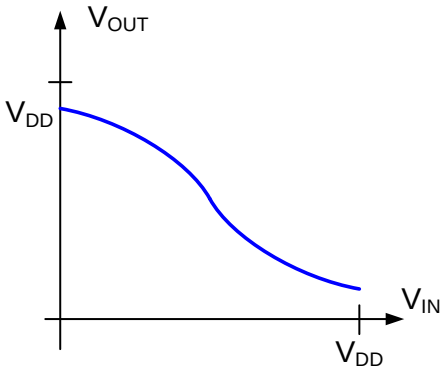


Figure 2-5: General transfer characteristics of an inverter

When two inverters are cascaded, the general transfer characteristics of a two-inverter pair can be obtained as shown in Figure 2-6. There are 3 possible transfer curves that can be realized depending on the device sizing. The dashed line is the line of unit slope corresponding to $V'_{OUT} = V_{IN}$, such that any intersection points between the transfer curves and the unity-slope line depict the possible operating points when the V_{IN} node is connected to the V'_{OUT} node.

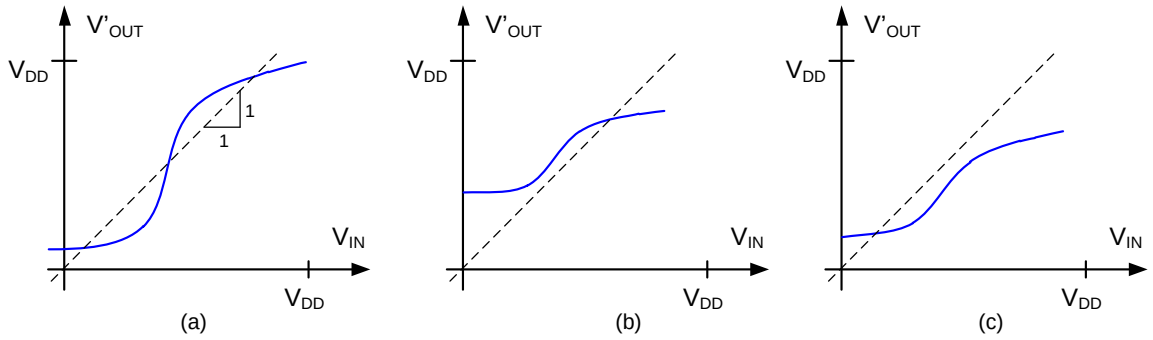


Figure 2-6: General transfer characteristics of 2 inverters pair

In the scenario of Figure 2-6(a), there exist 3 intersection points on the unity-slope line. The top and bottom intersection points occur when the loop gain is less than 1 and are recognized as stable equilibrium points. The intersection point in the middle occurs when the loop gain is more than 1. When operating at this point, the circuit is metastable and the point

is not a stable equilibrium point. In the scenario of Figure 2-6(b) and (c), there is only one intersection point and that it occurs when the loop gain is less than 1. In these scenarios, the circuit will only have one stable equilibrium point.

The notion of a startup circuit is to modify the circuit in such a way that the transfer characteristics are unchanged when operating near the desired operating point [**21**] but whereby all other equilibrium points, that is both stable and metastable operating points, are eliminated. This concept is illustrated in Figure 2-7.

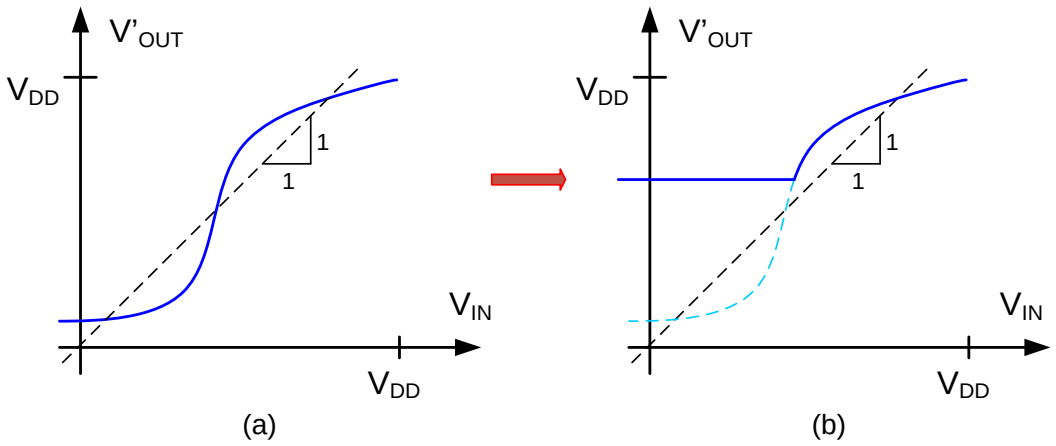


Figure 2-7: Transfer characteristics of a CMOS reference generator where start-up circuit preserves characteristics in region of desirable stable equilibrium point.

There are many ways to design a startup circuit to guarantee a single stable equilibrium point. The condition imposed that the startup circuit must not interfere with the normal operation of the circuit at the desired operating point may be relaxed when it is recognized the designer is free to take advantage of the start-up circuit to achieve better performance from the overall circuit. Ultimately, the goal with the startup circuit is thus to guarantee that the circuit has a single stable equilibrium point. In reality, most reported

startup circuits are designed to have the properties depicted in Figure 2-7 though they are seldom if ever presented from this viewpoint.

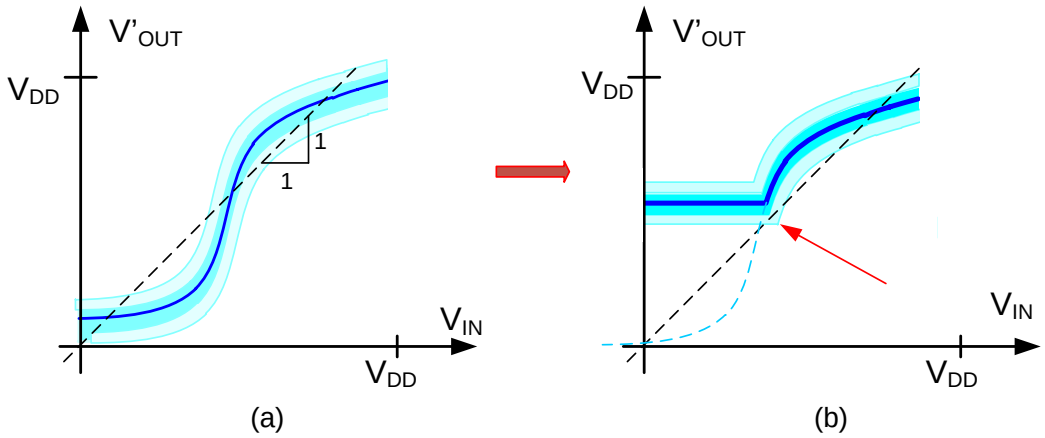


Figure 2-8: Parameter variations effect on transfer characteristics of a CMOS reference generator with start-up circuit

Process, voltage and temperature (PVT) induced parameter variations may cause significant shifts in the transfer characteristics of a reference generator as shown by the light blue shadows around the typical transfer characteristics in Figure 2-8(a). It is essential that the startup circuit be sufficiently robust so that under all acceptable PVT variations, a single stable equilibrium point is maintained. Figure 2-8(b) shows a situation where a start-up circuit is effective under typical conditions (illustrated by the dark blue curve) but where under PVT variations, additional equilibrium points reappear. The reappearance of undesirable equilibrium points are shown by the red arrow in Figure 2-8(b).

It can be shown that the circuit of Fig. 2-3 has three equilibrium points when designed to operate as a reference generator and only one of these is the desired stable equilibrium point. A single-transistor startup circuit as suggested in [**12**] can be used to guarantee a single operating point for this circuit as shown in Figure 2-9.

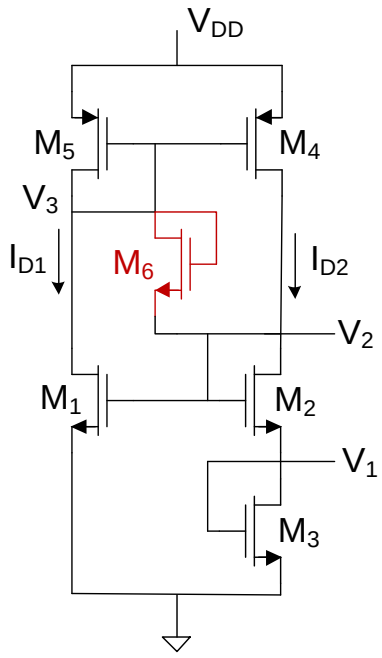


Figure 2-9: Circuit with startup transistor M_6

The function of the startup transistor, M_6, can be qualitatively described as follows. As the circuit is operating in the near cut-off region, node V_2 will drop to near 0V while node V_3 will raise to near V_{DD}. When that occurs, the startup transistor M_6 will be turned on. The current conduction through M_6 will sink the current from M_5 and source the current through M_2, effectively pulling node V_2 up and pulling node V_3 down. It is thus argued that the transistor M6 prevents the circuit from operating at either the metastable operating point or at the undesired unstable equilibrium point. And, when the circuit starts operating at the desired stable equilibrium point, the transistor M_6 turns off, thus providing no effect on the desired operation of the circuit. As a result, the circuit will always operate in strong inversion and only to have one desired stable equilibrium point.

2.5 DESIGN OF A P-TYPE REVERSE WIDLAR TEMPERATURE SENSOR

It is well-known that interchanging p-channel transistors with n-channel transistors and interchanging V_{DD} with V_{SS} in most MOS circuits results in a counterpart circuit that has properties similar to that of the original circuit. This concept applies to the bias generator circuits of Figure 2-2.

Following this approach, a P-channel version of the 5-transistors reverse Widlar temperature sensor is shown in Figure 2-10. In the P-channel version, the outputs will be measured relative to V_{DD} and the supply voltage independence will be relative to V_{SS} rather than to V_{DD}. This distinction only has bearing on specifying the supply voltage sensitivity so for notational convenience, simulation results will be presented for output voltages of this circuit relative to V_{SS}. The sensor has been implemented in 1P6M 0.18µm process with supply voltage of 1.8V [**17**] [**18**].

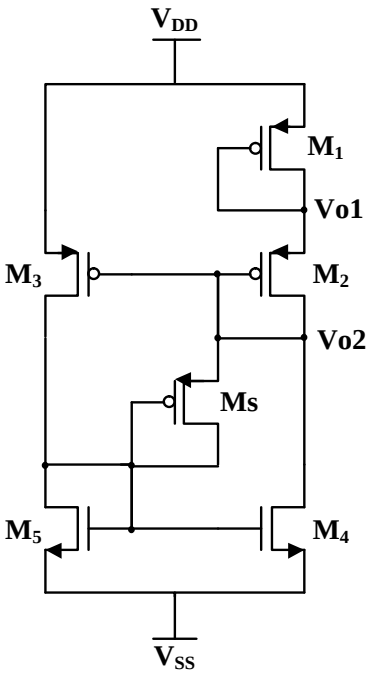


Figure 2-10: Schematic of a P-type reverse Widlar temperature sensor

The sensor was designed to operate in the temperature range between -20°C and 100°C. The nonlinear error of the sensor, expressed in °C, is the difference in the measured temperature and the end-point fit line temperature. The temperature integral nonlinearity error (TINL) in °C at the output node of the sensor is defined as

$$TINL = \left[\max_{100^oC<T<150^oC} \left| V_o(T) - V_{OFIT}(T) \right| \right] \left(\frac{50^oC}{V_O(150^oC) - V_O(100^oC)} \right) \qquad (2.22)$$

where $V_{OFIT}(T)$ is the output end-point fit line to the two points V_O(-20°C) and V_O(100°C).

The goal of this design is to achieve temperature INL of less than 1°C over the temperature range from -20°C to 100°C.

The transistors sizes used in this design are given in Table 2-1. Although not shown in Figure 2-10, transistor M_2 has its source tied up to its own n-well (body) directly so that V_{BS2}=0.

Table 2-1: Transistors size for P-type reverse Widlar temperature sensor

Transistor	M_1	M_2	M_3	M_4	M_5	M_S
Size (µm)	$\frac{W_1}{L_1} = \frac{4 \times 8.32}{0.72}$	$\frac{W_2}{L_2} = \frac{4}{0.36}$	$\frac{W_3}{L_3} = \frac{1.2}{1.5}$	$\frac{W_4}{L_4} = \frac{6 \times 1.4}{0.4}$	$\frac{W_5}{L_5} = \frac{6 \times 1.4}{0.4}$	$\frac{W_S}{L_S} = \frac{0.36}{12}$

2.5.1 Simulation Results

To gain insight into the effects of process and supply voltage variations on the circuit performance, the circuit was simulated at typical (denoted as TT) and over different process corners (FF: Fast NMOS Fast PMOS, SS: Slow NMOS Slow PMOS, FS: Fast NMOS Slow

PMOS, SF: Slow NMOS Fast PMOS) and with ±10% variation around the nominal V_{DD} of 1.8V. The simulation results are shown in Figure 2-11.

It can be observed from Figure 2-11(a) that the slope of all curves over process and over supply variations is about -1.14mV/°C with a variation in slope at TT over process and over supply voltage variations of ±10% that varies from -1.08mV/°C to -1.17mV/°C. If uncorrected, over a temperature range from T_{MIN} to T_{MAX}, the change in the output voltage could be as large as

$$\Delta V_{OUT} = \Delta m_{MAX} \bullet \frac{T_{MAX} - T_{MIN}}{2} \tag{2.23}$$

where Δm_{MAX} is the change in slope from nominal. The corresponding temperature error would be

$$\Delta T = \frac{\Delta m_{MAX}}{m_{NOM}} \bullet \frac{T_{MAX} - T_{MIN}}{2} \tag{2.24}$$

where m_{NOM} is the nominal slope.

Over a 120°C operating range, this would correspond to a temperature error of $\Delta T = \frac{0.09mV}{1.14mV} \bullet \frac{120}{2} = 4.74^{o}C$. If operating over a 30°C temperature range which is more typical of power management applications, this error would be reduced to $\Delta T = \frac{0.09mV}{1.14mV} \bullet \frac{30}{2} = 1.18^{o}C$. Both errors are unacceptably large. However, the slope error due to process variations in the slope can be calibrated out with a two-point calibration or significantly reduced with a batch calibration. Simulation results show that the slope error

due to process variations with a fixed supply voltage vary from -1.142mV/°C to -1.139mV/°C. This corresponds to a temperature error that can be calibrated out of $\Delta T = \frac{0.003mV}{1.14mV} \bullet \frac{120}{2} = 0.16^{o}C$ over a 120°C operating range and a temperature error of $\Delta T = \frac{0.003mV}{1.14mV} \bullet \frac{30}{2} = 0.04^{o}C$ over a 30°C range. Simulation results show a worst-case slope variation with supply variations occurs at FF of $\Delta T = \frac{0.017mV}{1.15mV} \bullet \frac{120}{2} = 0.89^{o}C$ over a 120°C operating range and a temperature error of $\Delta T = \frac{0.017mV}{1.15mV} \bullet \frac{30}{2} = 0.22^{o}C$ over a 30°C range. Over the 120°C operating range, this error of 0.89°C is a significant contributor to the overall error budget since it cannot be calibrated out. Over the 30°C operating range, it does not cause a significant loss in accuracy.

From Figure 2-11(a), it is apparent that there is a significant variation of output voltage with process and with supply voltages. At a fixed supply voltage, the variation in the output with process is approximately 100mV. With a temperature of about -1.14mV/°C, this variation in output would cause a temperature error of up to 88°C. This error is so large that the temperature sensor would be of almost no use. However, a single-point calibration at any temperature can be used to shift the curves up or down to remove the process dependence of this error and it will be assumed that a single-point calibration will be used to eliminate this error.

With a fixed supply voltage, the simulation results show that the maximum temperature nonlinear error at typical conditions is 0.0523°C over the temperature range

from -20°C and 100°C; while the worst-case maximum temperature error of 0.702°C occurs at the FF corner with a high voltage of 1.98V. This temperature error is very small and is much smaller than any experimental results that have been presented for on-chip temperature sensors.

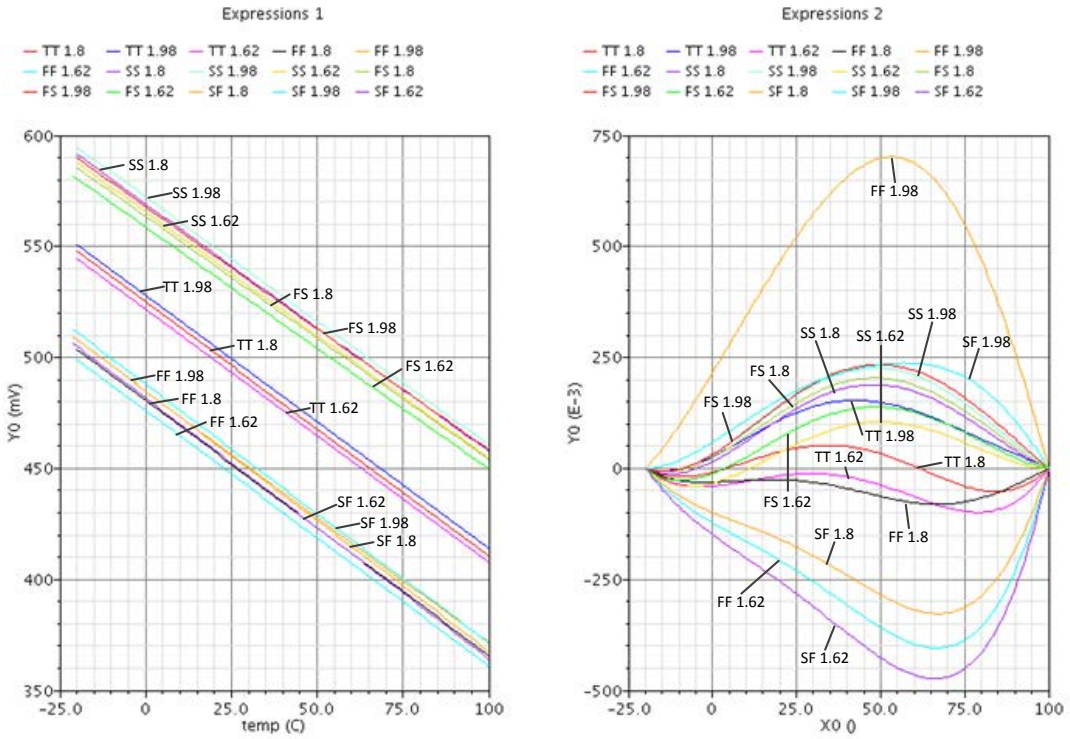


Figure 2-11: Simulated 5T (a) output voltage and (b) temperature INL at different process corners and ±10% variation over nominal V_{DD} of 1.8V

The transfer characteristics of the 5-transistors reverse Widlar temperature sensor after breaking the loop at node V_{O2} were obtained by simulation over all process corners and with VDD variation of ±10%. Results both with and without the startup circuit were obtained. These results are shown in Figure 2-12. Looking at the family of curves, it is apparent that without a startup circuit, one or more of the transfer characteristics have three crossings of the unity slop line. For example, at the SF corner, the circuit will have 2 stable equilibrium points and 1 metastable operating point. Hence a startup circuit is required to

prevent the circuit from having multiple stable equilibrium operating points. It also follows from the simulation results in Figure 2-12 that with the startup circuit, there is only a single stable equilibrium point at TT or at any process corners.

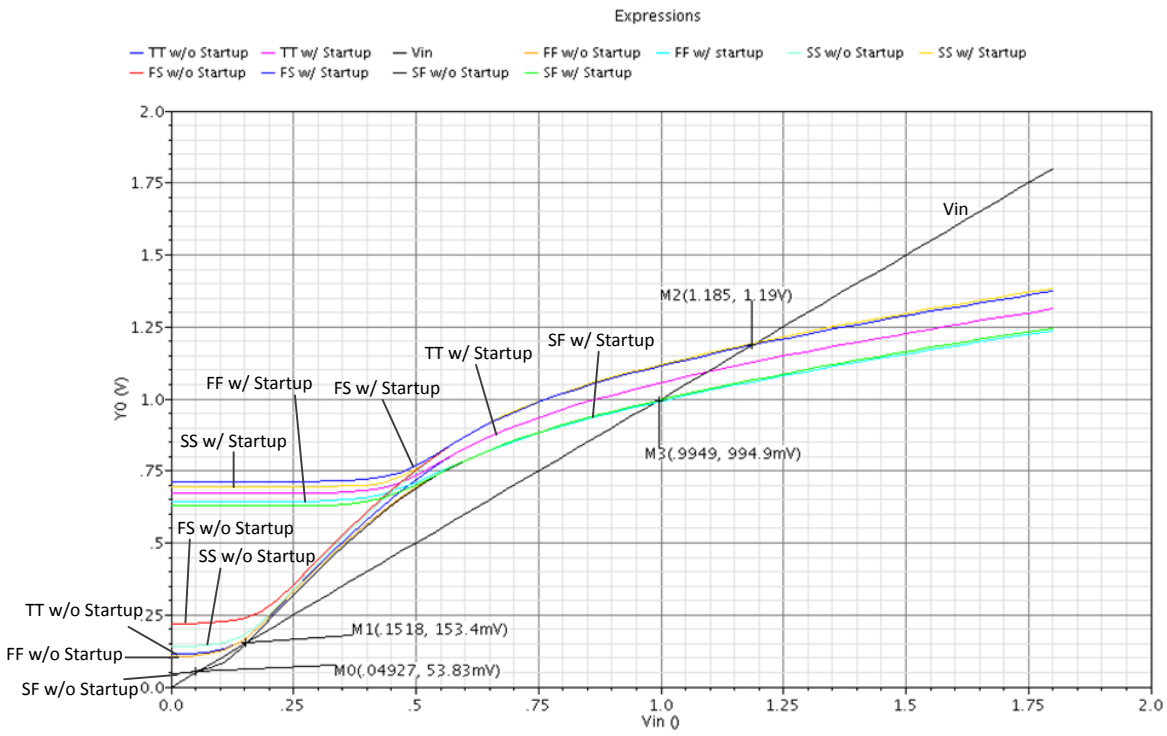


Figure 2-12: Simulated transfer characteristics of the 5T reverse Widlar temperature sensor

If the supply voltage itself changes, possibly due to changes in loading, possibly due to a temperature dependence of the supply voltage, or possibly due to noise on the supply, these supply voltage changes will also be interpreted as a temperature measurement errors. And, unlike the process variation shifts, these variations cannot be calibrated out. At typical conditions, if VDD varies ±10% in real-time, the simulation results in Figure 2-11 show that the output voltage variation will be 6.72mV. This output variation is almost entirely due to the output conductance effects of the devices. With a nominal temperature coefficient of -1.141mV/°C, this would cause an additional temperature error of 5.89°C. This error would

completely dominate the nonlinear error of 0.0523°C attributable to device nonlinearity. From a slightly different perspective, the ±10% supply voltage change of 360mV results in an output change of 6.72mV which corresponds to a supply sensitivity of the output of about 0.019. Although the supply sensitivity is low, it is still much too high to achieve good accuracy of the temperature sensor if the supply voltage is allowed to change by ±10%. From a practical viewpoint, either the variability of the supply voltage needs to be reduced or the circuit needs to be modified to make the supply voltage sensitivity significantly smaller. That latter can be achieved by using cascoding. A straightforward inspection on the structure of the 5-transistors circuit reveals the voltage headroom is the difference between the actual supply voltages and the sum of three excess bias voltages and two threshold voltage drops. At the nominal supply voltage of 1.8V at TT, it can be shown that there is enough headroom for full cascoding of this structure. But at the SS process corner with a -10% drop in supply voltage, there is not enough headroom for cascoding of the 5-transistors temperature sensor. The issue of cascoding is discussed in Appendix 2A and in Chapter 3.

In addition, the noise performance for the 5-transistors temperature sensor is of concern because of the following reasons. Firstly, the output signal level due to small temperature-voltage coefficient (slope) is relatively small over the temperature range of 120°C. This leads to low signal-to-noise ratio (SNR), where the output node is more susceptible to noise. Secondly, the single-ended output of the circuit causes the common-mode output noise to persist. Conventional differential mode cancellation techniques are not feasible and cannot be applied to this design. Hence, the only way possible to reduce noise is

to increase the channel length. This then becomes a trade-off problem to the small-area design.

The simulated noise performance in frequency domain is shown in Figure 2-13. Detailed analytical derivations are shown in Appendix 2B.

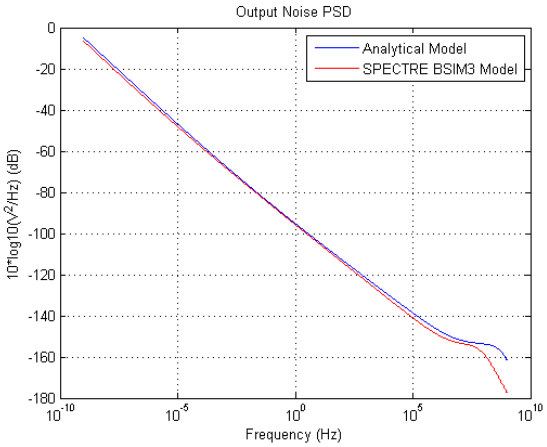


Figure 2-13: Output noise power spectral density for 5T P-type temperature sensor

The time-domain noise performance plot is then obtained by taking the integral of the output noise PSD from 1GHz to range of frequencies corresponding to the equivalent time periods. The results are shown in Figure 2-14.

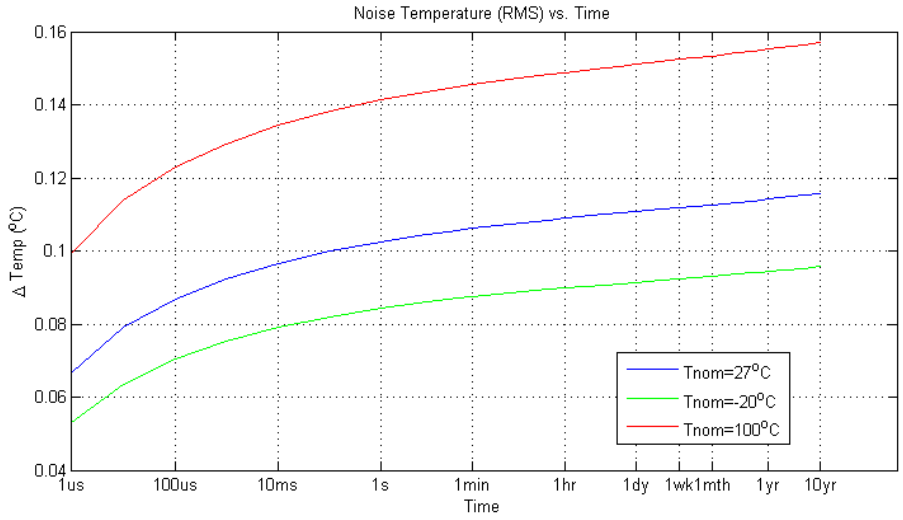


Figure 2-14: RMS noise temperature of the 5T P-type temperature sensor in time domain

From the plot, it can be inferred that the 5T temperature sensor will have RMS noise temperature of 0.26°C over the period of 10 years. This is well below the design goal to attain temperature sensing performance with less than 1°C error.

The power dissipation of this temperature sensor is about 31uW at room temperature if the sensor is always on. This power dissipation is very small but could be reduced much further if the temperature sensor were only turned on when a temperature measurement was required. The area required for the temperature sensor is estimated at about 320 μm^2 which is very small. Simulation results are summarized in Table 2-2.

Table 2-2: Summary of performance for 5T P-type reverse Widlar temperature sensor

Specification	**Performance**
Process	0.18μm
Voltage Supply	1.8V
Temperature Range	-20~100˚C
Parameter	**5T P-Type**
Layout Estimated Area (μm^2)	321
Nominal power consumption (μW)	30.6
Temperature Coefficient (mV/ ˚C)	-1.141
Max. Temp. INL (˚C) at Typical	0.0523
Max. Temp. INL (˚C) at Worst Case	0.702
Supply Sensitivity at Typical (˚C)	5.89

2.6 CONCLUSION

An analysis of a 5-transistor reverse Widlar CMOS current reference was presented. This structure has a low V_{DD} sensitivity and if designed properly, it can serve as a compact temperature sensor with good temperature linearity. Based on previous work [**17**], a P-Type 5-transistors reverse Widlar temperature sensor was designed. The circuit demonstrates good

overall temperature linearity of less than 1°C with low power consumption and small layout area. Although the circuit has low V_{DD} sensitivity, under supply voltage variations of ±10%, the supply voltage variations will be interpreted as an unacceptably large temperature error and this temperature error cannot be calibrated out with either a single-point or even a two-point calibration. Since the V_{DD} sensitivity error is almost entirely due to the finite output impedance of the MOS devices, cascoding can be used to reduce this error and it is easy to show that cascoding will reduce this sensitivity enough so that the resultant temperature error is negligible. However, in the 1.8V process considered in a design presented in this Chapter, there is not enough headroom to keep all devices in saturation over process, temperature, and supply voltage variations. In the next chapter, a new circuit structure for temperature sensing applications will be introduced that has enough headroom for full cascoding in even smaller feature size processes.

APPENDIX 2A POWER SUPPLY EFFECTS ON INTEGRATED TEMPERATURE SENSORS

Adapted work by R. Geiger March 7, 2011

Although the goal has been to build VDD-insensitive temperature sensors, reality remains that the supply voltage does have some effect on the output voltage. In this section an analytical formulation of the effects of the supply voltage on the temperature output will be discussed. Specifically, analytical expressions for the transfer function from the supply node to the output node will be derived. This ratio is the sensitivity to the supply voltage that was discussed in Chapter 2. In this appendix, a script font will be used to denote the small signal voltages. So, for example, with this convention, V_{DD} refers to the actual supply voltage but $\mathcal{v}_{DD}$ refers to the small-signal supply voltage.

Consider initially the temperature sensor shown in Figure 2-15. In this figure the Widlar resistor is used though the analysis can be readily extended when the resistor is replaced with a diode-connected transistor.

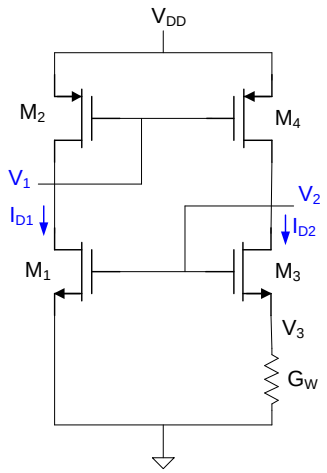


Figure 2-15: Basis VDD-independent temperature sensor

The small signal equivalent circuit of this temperature sensor is shown in Figure 2-16.

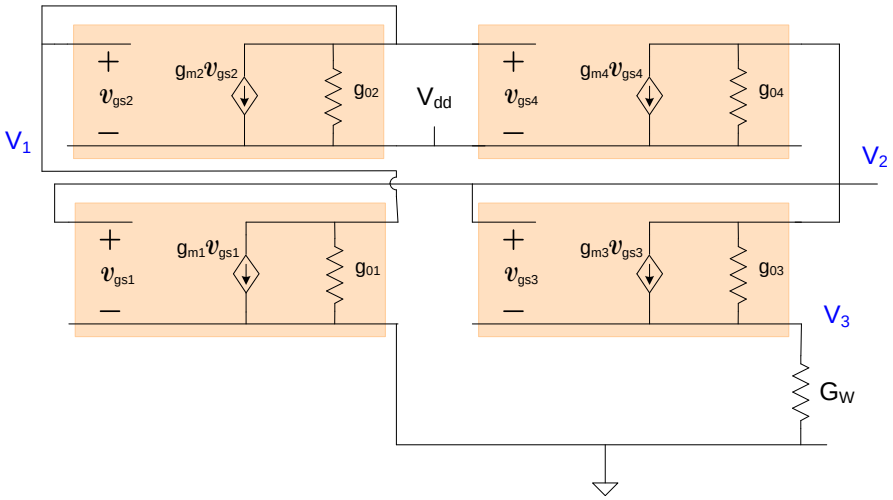


Figure 2-16: Small-signal equivalent temperature sensor of Figure 2-15

If follows from Kirchhoff's Current Law (KCL) that

$$\left.\begin{aligned} V_1(g_{o1}+g_{o2})+g_{m1}V_{gs1}+g_{m2}V_{gs2}&=g_{o2}V_{DD}\\ V_2(g_{o3}+g_{o4})+g_{m4}V_{gs4}+g_{m3}V_{gs3}&=V_3g_{o3}+g_{o4}V_{DD}\\ V_3(g_{o3}+G_W)&=g_{o3}V_2+g_{m3}V_{gs3}\end{aligned}\right\} \tag{2.25}$$

In these equations, the gate-source voltages are given by

$$\left.\begin{aligned} V_{gs1}&=V_2\\ V_{gs2}&=V_1-V_{DD}\\ V_{gs3}&=V_2-V_3\\ V_{gs4}&=V_1-V_{DD}\end{aligned}\right\} \tag{2.26}$$

Substituting into (2.25), three equations are obtained

$$\left.\begin{aligned} V_1(g_{o1}+g_{o2})+g_{m1}V_2+g_{m2}(V_1-V_{DD})&=g_{o2}V_{DD}\\ V_2(g_{o3}+g_{o4})+g_{m4}(V_1-V_{DD})+g_{m3}(V_2-V_3)&=V_3g_{o3}+g_{o4}V_{DD}\\ V_3(g_{o3}+G_W)&=g_{o3}V_2+g_{m3}(V_2-V_3)\end{aligned}\right\} \tag{2.27}$$

These can be rewritten as

$$\left.\begin{aligned} &V_1\left(g_{o1}+g_{o2}+g_{m2}\right)+V_2 g_{m1}=V_{DD}\left(g_{m2}+g_{o2}\right)\\ &V_2\left(g_{o3}+g_{o4}+g_{m3}\right)+V_1 g_{m4}=V_3\left(g_{o3}+g_{m3}\right)+V_{DD}\left(g_{m4}+g_{o4}\right)\\ &V_3\left(g_{o3}+G_W+g_{m3}\right)=V_2\left(g_{m3}+g_{o3}\right)\end{aligned}\right\} \tag{2.28}$$

Eliminating v_1 and v_3, we obtain the single equation

$$\begin{aligned} &V_2\left(g_{o3}+g_{o4}+g_{m3}\right)+V_{DD}\frac{g_{m4}\left(g_{m2}+g_{o2}\right)}{\left(g_{o1}+g_{o2}+g_{m2}\right)}-V_2\frac{g_{m1}g_{m4}}{\left(g_{o1}+g_{o2}+g_{m2}\right)}=\\ &V_2\frac{\left(g_{m3}+g_{o3}\right)}{\left(g_{o3}+G_W+g_{m3}\right)}\left(g_{o3}+g_{m3}\right)+V_{DD}\left(g_{m4}+g_{o4}\right)\end{aligned} \tag{2.29}$$

This can be solved to obtain the expression

$$\frac{V_2}{V_{DD}}=\frac{\left[\dfrac{g_{m4}g_{o1}+g_{m2}g_{o4}+g_{o4}\left(g_{o1}+g_{o2}\right)}{g_{o1}+g_{o2}+g_{m2}}\right]}{\left[\dfrac{\left(g_{o3}+g_{m3}\right)\left(g_{o4}+G_W\right)+g_{o4}G_W}{\left(g_{o3}+g_{m3}+G_W\right)}-\dfrac{g_{m1}g_{m4}}{\left(g_{o1}+g_{o2}+g_{m2}\right)}\right]} \tag{2.30}$$

It is difficult to get much insight into how large this gain or attenuation is because of the high level of interdependence between the small signal variables in (2.30). It will now be assumed that all output conductances are small compared to any transconductances in each of the three ratios given in (2.30). Of course, there is some risk at making this assumption since a difference of two functions appears in the denominator of (2.30). So, after making this assumption, it will be necessary to show that the difference in the denominator of (2.30) is large compared to the effects of the output conductances.

With this assumption, it follows that

$$\frac{V_2}{V_{DD}} \simeq \frac{\left[\frac{g_{m4}g_{o1} + g_{m2}g_{o4}}{g_{m2}}\right]}{\left[\frac{(g_{m3})(G_W)}{(g_{m3} + G_W)} - \frac{g_{m1}g_{m4}}{(g_{m2})}\right]} \tag{2.31}$$

A relation between the large signal and small signal parameters will now be made. Specifically, for each device it will be assumed that

$$\begin{aligned} g_o &= \lambda I_{DQ} \\ g_m &= \frac{2I_{DQ}}{V_{EB}} \end{aligned} \tag{2.32}$$

Now define the mirror gain of the p-channel current mirror to be M. It thus follows that

$$V_{3Q}G_W = MI_{D1Q} \tag{2.33}$$

The excess bias voltages of the n-channel transistors can be expressed as

$$\begin{aligned} V_{EB1} &= V_{2Q} - V_{Tn1} \\ V_{EB3} &= V_{2Q} - V_{3Q} - V_{Tn3} \end{aligned} \tag{2.34}$$

Substituting from (2.32), (2.33) and (2.34) into (2.31) yields

$$\frac{V_2}{V_{DD}} \simeq \frac{\lambda_1 + \lambda_4}{\left[\frac{2}{2V_{EB1} - V_{EB3}} - \frac{2}{V_{EB1}}\right]} \tag{2.35}$$

For convenience define the parameter φ as

$$\phi = \frac{V_{EB3}}{V_{EB1}} \tag{2.36}$$

It thus follows that

$$\frac{V_2}{V_{DD}} \simeq \frac{(\lambda_1 + \lambda_4)V_{EB1}}{-2\left(\frac{1-\phi}{(2-\phi)}\right)} \tag{2.37}$$

The parameter φ is generally much less than 1 so the denominator in (2.37) is not small justifying the assumption that we could neglect all g_o terms in the denominator of (2.30).

It might be useful to provide a bit more insight into what (2.37) shows.

$$\frac{V_2}{V_{DD}} \simeq \frac{(\lambda_1 + \lambda_4)V_{EB1}}{-2\left(\frac{1-\phi}{(2-\phi)}\right)} = \left[\frac{\phi-2}{1-\phi}\right]\frac{(\lambda_1 + \lambda_4)I_{D1Q}V_{EB1}}{2I_{D1Q}} \tag{2.38}$$

Assuming that $\lambda_1=\lambda_4=\lambda$, it follows that

$$\frac{V_2}{V_{DD}} \simeq \left[\frac{\phi-2}{1-\phi}\right]\frac{\left(2\lambda I_{D1Q}\right)}{\left(\frac{2I_{D1Q}}{V_{EB1}}\right)} \tag{2.39}$$

The linear dependence on the output conductance parameter is apparent from this expression. And the designer has considerable control over this ratio through judicious choices of V_{EB1}, V_{EB2} and V_{EB3}. However, these parameters also affect the linearity of the temperature sensor and are constrained by headroom and power limitations.

The ratio in (2.39) can also be expressed in terms of small signal parameters

$$\frac{V_2}{V_{DD}} \simeq 2\left[\frac{\phi-2}{1-\phi}\right]\frac{g_{o1}}{g_{m1}} \tag{2.40}$$

The magnitude of the coefficient of g_{o1}/g_{m1} is shown in the following figure.

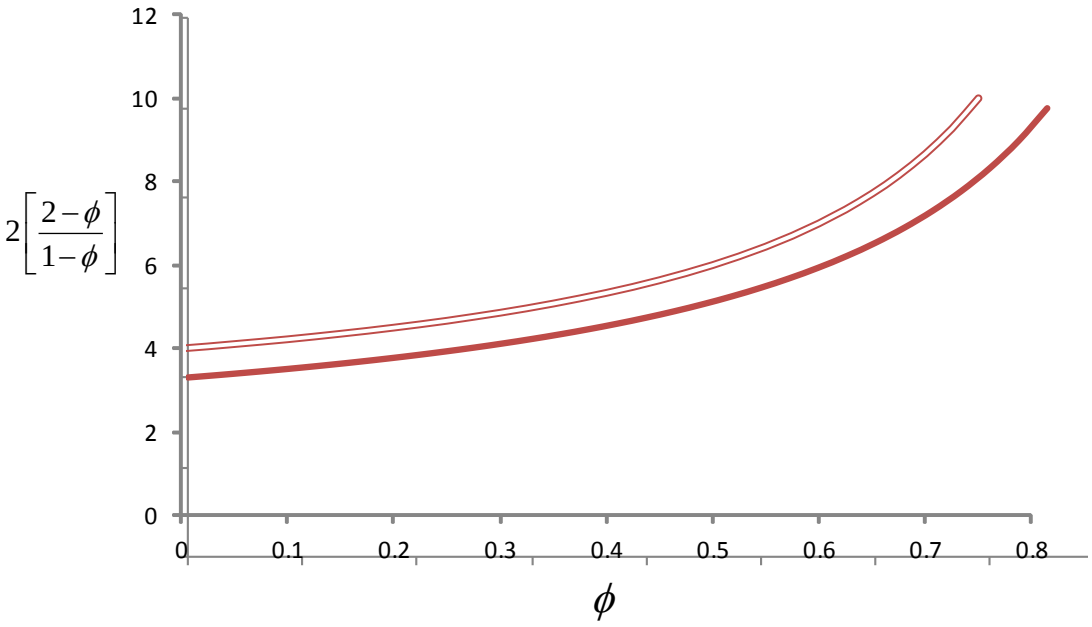


Figure 2-18: Magnitude of coefficient in (2.40)

Equations (2.39) and (2.40) are analytical expressions for the sensitivity of the output with respect to the supply voltage.

The issue of cascoding also deserves attention. A cascoded structure is shown in Figure 2-19 where the transistors M_1 and M_4 have been cascoded.

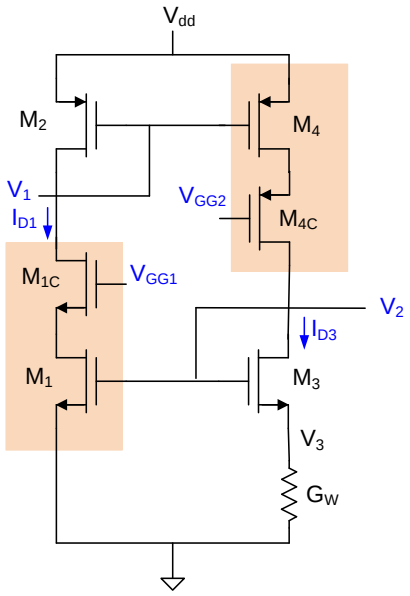


Figure 2-19: Cascoded reference generator

The cascoded transistor pairs have an equivalent small-signal transconductance and output conductance given by

$$g_{mcc} = g_m$$
$$g_{occ} = g_0\left(\frac{g_{0c}}{g_{mc}}\right) \tag{2.41}$$

It thus follows directly from (2.31) that the output voltage for the cascoded structure can be expressed as

$$\frac{V_2}{V_{DD}} \simeq \frac{\left[\dfrac{g_{m4}g_{o1}\left(\dfrac{g_{o1c}}{g_{m1c}}\right)+g_{m2}g_{04}\left(\dfrac{g_{o4c}}{g_{m4c}}\right)}{g_{m2}}\right]}{\left[\dfrac{(g_{m3})(G_W)}{(g_{m3}+G_W)}-\dfrac{g_{m1}g_{m4}}{(g_{m2})}\right]} \tag{2.42}$$

In terms of the large signal operating parameters, it follows that

$$\frac{V_2}{V_{DD}} \simeq \frac{\left(\lambda_1\lambda_{1C}V_{EB1c} + \lambda_4\lambda_{4C}V_{EB4c}\right)V_{EB1}}{-2\left(\frac{1-\phi}{(2-\phi)}\right)} \tag{2.43}$$

As expected, the cascoding reduces the gain from v_{DD} significantly.

Assuming that $\lambda_1=\lambda_4=\lambda_{1C}=\lambda_{4C}=\lambda$, and $V_{EB1}=V_{EB1C}$ and $V_{EB4}=V_{EB4C}$, it follows that

$$\frac{V_2}{V_{DD}} \simeq 2\left[\frac{\phi-2}{1-\phi}\right]\left(\frac{g_{o1}}{g_{m1}}\right)^2 \tag{2.44}$$

The gain from V_{DD} is decreased by approximately a factor of g_{o1}/g_{m1}.

The issue of the effect of the power supply on the dc biasing voltages for the cascode transistors does deserve attention. It can be shown that the gain from the biasing voltage on the gates of the cascode transistors to the output is quite small. Likewise, it is rather easy to design the bias generator so that the effects of the supply voltage on the gate voltage of the cascode transistors are also small. Thus, the overall gain from the power supply to the output through the biasing transistors of the cascode devices will also be small, provided that all transistors are operating well in the saturation region.

APPENDIX 2B NOISE ANALYSIS ON REVERSE WIDLAR TEMPERATURE SENSOR

As with any analog circuit, the effects of noise on the performance of the temperature sensor must be considered as part of the design process. In the case of a temperature sensor where temperature information is encoded in an analog output voltage, the noise voltage at the output should ultimately be converted into a "temperature" noise.

The output noise voltage is characterized by a power spectral density, S_P. The RMS output noise voltage attributed to noise in the frequency band from f_1 to f_2 is given by the expression.

$$V_{[f_1,f_2]} = \sqrt{\int_{f_1}^{f_2} |S_P| df} \tag{2.45}$$

The power spectral density of each transistor is comprised of a thermal-noise region and a 1/f noise region. The transition between these regions is termed the noise corner frequency for the transistor. The corner frequency, in general, will be different for n-channel and p-channel devices with the corner frequency occurring at lower frequencies for p-channel devices in most processes.

In the BSIM4 Level 0 model as given in [**19**], the 1/f noise current spectral density of a MOS transistor is given by

$$S_{1/f} = \frac{K_F I_{ds}^{AF}}{C_{ox} L_{eff}^2 f^{EF}} \tag{2.46}$$

where AF and EF are usually equal to 1, K_F is the empirical flicker noise constant, I_{DS} is the quiescent current level, C_{ox} is the gate oxide capacitance density, L_{eff} is the effective transistor length, and f is frequency.

In contrast, there is nearly universal agreement in how the power spectral density of the thermal noise current should be modeled. The power spectral density of the thermal noise current is often expressed in terms of the small signal transconductance gain of the MOS transistor, g_m, and is expressed as

$$S_n = \frac{8}{3} kTg_m \tag{2.47}$$

where T is the temperature in Kelvin and where k is Boltzmann's constant.

The small signal transconductance parameter g_m can be expressed in terms of the quiescent operating point in different equivalent ways but for what follows here, g_m will be expressed as

$$g_m = \frac{2I_{ds}}{V_{EB}} \tag{2.48}$$

The mechanisms that contribute to 1/f noise and that contribute to thermal noise are assumed to be uncorrelated. Thus the spectral density of the drain noise current in a MOS transistor is the sum of the spectral densities of the thermal noise and 1/f noise and can be expressed as

$$S_n = \frac{8}{3} kTg_m + \frac{K_F I_{ds}^{AF}}{C_{ox} L_{eff}^2 f^{EF}} \tag{2.49}$$

The 1/f noise corner is the frequency where the 1/f noise equals the thermal noise. It thus follows from (2.48) and (2.49) that the noise corner frequency, f_{NC} is given by

$$f_{NC} = \frac{\frac{K_F I_{ds}^{AF}}{C_{ox} L_{eff}^2}}{\frac{8kT}{3} g_m} = \frac{3}{16kT} \frac{K_F V_{EB}}{C_{ox} L_{eff}^2} \tag{2.50}$$

From this expression, it is apparent that the noise corner decreases with increasing gate length and is also dependent upon the excess bias voltage, V_{EB}.

Although thermal noise and 1/f noise is present at all frequencies, at frequencies below the noise corner the 1/f noise dominates the thermal noise and at frequencies above the 1/f noise corner the thermal noise dominates the 1/f noise. The RMS drain noise current of a transistor contributed by frequencies from a frequency f_{START} to ∞ can be expressed as

$$I_{RMS[f_{START},\infty]} = \sqrt{\int_{f_{START}}^{\infty} S_n df} \tag{2.51}$$

This can be written as

$$I_{RMS[f_{START},\infty]} = \sqrt{\int_{f_{START}}^{f_{NCn}} S_n df + \int_{f_{NCn}}^{\infty} S_n df} \tag{2.52}$$

From the observation that 1/f noise dominates at frequencies below the noise corner and that thermal noise dominates at frequencies above the noise corner, the noise current can be approximated by the expression

$$I_{RMS[f_{START},\infty]} \simeq \sqrt{\int_{f_{START}}^{f_{NC}} \frac{K_F I_{ds}^{AF}}{C_{ox} L_{eff}^2 f^{EF}} df + \int_{f_{NCn}}^{\infty} \frac{8}{3} kT g_m \, df} \tag{2.53}$$

This expression modestly under-estimates the total RMS noise current but the estimation error is quite small. From this expression, the first integral is the contribution of the 1/f noise and the second integral is the contribution of the thermal noise to the overall RMS noise current. We can thus write the expressions

$$I_{RMS,Flicker[f_{START},\infty]} \simeq \sqrt{\int_{f_{START}}^{f_{NC}} \frac{K_F I_{ds}^{AF}}{C_{ox} L_{eff}^2 f^{EF}} df} \tag{2.54}$$

and

$$I_{RMS-Thermal[f_{START},\infty]} \simeq \sqrt{\int_{f_{NCn}}^{\infty} \frac{8}{3} kTg_m \, df} \tag{2.55}$$

and observe from (2.53), (2.54), and (2.55) that

$$I_{RMS[f_{START},\infty]} \simeq \sqrt{I^2_{RMS-Flicker[f_{START},\infty]} + I^2_{RMS-Thermal[f_{START},\infty]}} \tag{2.56}$$

This concept will be generalized to obtain approximations for the flicker noise voltage and the thermal noise voltage at the output of the temperature sensor.

If a circuit is comprised of k transistors, then the power spectral density of the output voltage can be expressed as

$$S_P = \sum_{i=1}^{k} \left| T_i(j\omega) \right|^2 S_{Pi} \tag{2.57}$$

where T_i is the transfer function from the i^{th} noise current source to the voltage output and S_{Pi} is the power spectral density of the i^{th} noise current source.

The total RMS noise voltage due to all frequency components above a frequency f_{START} is given by

$$V_{[f_{START},\infty]} = \sqrt{\int_{f_{START}}^{\infty} \left[\sum_{i=1}^{k} \left(\left| T_i(j\omega) \right|^2 S_i \right) \right] df} \qquad (2.58)$$

In a circuit comprised of k transistors, there may be k different noise corners, making it very difficult to break the integral in (2.58) up into different regions to obtain an analytical expression for the total RMS noise voltage. It is also difficult to analytically separate the 1/f noise contributions from the thermal noise contributions. For the purpose of determining an approximate expression for the combined 1/f noise contributions and the thermal noise contributions of all transistors, f_{MIN} and f_{MAX} are defined to be the minimum and the maximum of the noise corner frequencies of all k transistors. With this approach, a 1/f (flicker) noise voltage and a thermal noise voltage due to all transistors are defined by the expressions

$$V_{Flicker} \simeq \sqrt{\int_{f_{START}}^{f_{MAX}} \left(\frac{\sum_{i=1}^{k} \left| T_i(j\omega) \right|^2 H_i}{f} \right) df} \qquad (2.59)$$

$$V_{Thermal} \simeq \sqrt{\int_{f_{MIN}}^{\infty} \left(\sum_{i=1}^{k} \left| T_i(j\omega) \right|^2 \frac{8}{3} kTg_{m_i} \right) df} \qquad (2.60)$$

where

$$H_i = \frac{K_{Fi} I_{dsi}}{C_{ox} L_{eff_i}^2} \qquad (2.61)$$

From (2.60), the thermal noise voltage can be equivalently expressed in terms of quiescent current parameters by the expression

$$V_{Thermal} = \sqrt{\frac{16kT}{3} \int_{f_{MIN}}^{\infty} \left(\sum_{i=1}^{k} \left| T_i(j\omega) \right|^2 \frac{I_{dsi}}{V_{EBi}} \right) df} \tag{2.62}$$

The total RMS voltage in the frequency band from f_{START} to ∞ can thus be approximated by the expression

$$V_{RMS} = \sqrt{V_{Flicker}^2 + V_{Thermal}^2} \tag{2.63}$$

If the small error introduced by separating 1/f noise and thermal noise is neglected, this expression for $V_{Flicker}$ is a modest over-estimate for the contributions of the 1/f noise, and the expression for $V_{Thermal}$ is a modest over-estimate for the thermal noise.

In the context of a temperature sensor, what we are actually interested in is the RMS temperature error at the output due to the device noise in the MOS transistors. If γ is defined to be the nominal sensitivity of the output voltage to temperature, that is,

$$\gamma = \frac{\partial V_{OUT}}{\partial T} \tag{2.64}$$

Since the temperature sensors considered here are quite linear, it is not necessary to specify at which temperature the derivative in (2.64) is evaluated at. It thus follows that the RMS noise temperature at the output can be expressed as

$$T_{RMS} = \frac{1}{\gamma} \sqrt{V_{Flicker}^2 + V_{Thermal}^2} \tag{2.65}$$

FREQUENCY-DEPENDENT NOISE CHARACTERIZATION OF REVERSE WIDLAR SENSOR

The reverse Widlar temperature sensor is shown in Figure 2-20.

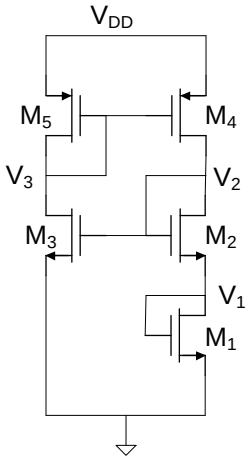


Figure 2-20: Reverse Widlar N-type temperature sensor

A small-signal equivalent circuit that includes the parasitic capacitances is shown in Figure 2-21. In this model, the parasitic capacitances on each node are the sum of the appropriate gate-source and diffusion capacitances. The gate-to-drain capacitances are assumed to be relatively small and thus are neglected.

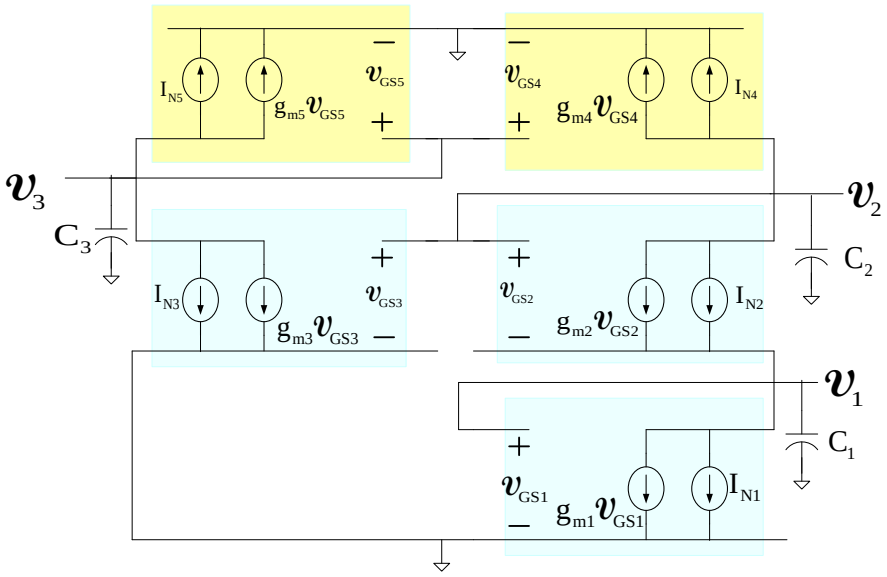


Figure 2-21: Frequency dependent noise model of the reverse Widlar temperature sensor

Summing currents at the three non-trivial nodes, the following set of equations are obtained.

$$\left.\begin{aligned}&\left(sC_1+g_{m1}\right)v_1+I_{N1}-g_{m2}\left(v_2-v_1\right)-I_{N2}=0\\&g_{m4}v_3+I_{N4}+sC_2v_2+g_{m2}\left(v_2-v_1\right)+I_{N2}=0\\&\left(sC_3+g_{m5}\right)v_3+I_{N5}+g_{m3}v_2+I_{N3}=0\end{aligned}\right\} \tag{2.66}$$

Eliminating v_3 yields

$$\left.\begin{aligned}&\left(sC_1+g_{m1}+g_{m2}\right)v_1-g_{m2}v_2+I_{N1}-I_{N2}=0\\&-g_{m4}\left(\frac{I_{N5}+g_{m3}v_2+I_{N3}}{sC_3+g_{m5}}\right)+I_{N4}+sC_2v_2+g_{m2}\left(v_2-v_1\right)+I_{N2}=0\end{aligned}\right\} \tag{2.67}$$

This simplifies to

$$\left.\begin{aligned}&\left(sC_1+g_{m1}+g_{m2}\right)v_1-g_{m2}v_2+I_{N1}-I_{N2}=0\\&v_2\left(\frac{sC_3+g_{m5}}{g_{m4}}\left(g_{m2}+sC_2\right)-g_{m3}\right)-v_1\frac{sC_3+g_{m5}}{g_{m4}}g_{m2}+\frac{sC_3+g_{m5}}{g_{m4}}\left(I_{N2}+I_{N4}\right)-\left(I_{N3}+I_{N5}\right)=0\end{aligned}\right\} \tag{2.68}$$

To find v_2, first eliminate v_1 to obtain

$$\begin{aligned}&v_2\left[\left(\frac{sC_3+g_{m5}}{g_{m4}}\left(g_{m2}+sC_2\right)-g_{m3}\right)\left(sC_1+g_{m1}+g_{m2}\right)-\frac{sC_3+g_{m5}}{g_{m4}}g_{m2}^2\right]+\frac{sC_3+g_{m5}}{g_{m4}}g_{m2}\left(I_{N1}-I_{N2}\right)\\&+\frac{sC_3+g_{m5}}{g_{m4}}\left(sC_1+g_{m1}+g_{m2}\right)\left(I_{N2}+I_{N4}\right)-\left(sC_1+g_{m1}+g_{m2}\right)\left(I_{N3}+I_{N5}\right)=0\end{aligned} \tag{2.69}$$

It thus follows that v_2 can be expressed as

$$v_2 = \frac{-\left(\frac{sC_3+g_{m5}}{g_{m4}}g_{m2}\right)I_{N1}+\left(\frac{sC_3+g_{m5}}{g_{m4}}g_{m2}-\frac{sC_3+g_{m5}}{g_{m4}}(sC_1+g_{m1}+g_{m2})\right)I_{N2}-(sC_1+g_{m1}+g_{m2})\left(\frac{sC_3+g_{m5}}{g_{m4}}I_{N4}-I_{N3}-I_{N5}\right)}{\left[\left(\frac{sC_3+g_{m5}}{g_{m4}}(g_{m2}+sC_2)-g_{m3}\right)(sC_1+g_{m1}+g_{m2})-\frac{sC_3+g_{m5}}{g_{m4}}g_{m2}^2\right]}$$

(2.70)

To find v_1, first eliminate v_2 to obtain

$$\left[\left(\frac{sC_3+g_{m5}}{g_{m4}}(g_{m2}+sC_2)-g_{m3}\right)(sC_1+g_{m1}+g_{m2})-\frac{sC_3+g_{m5}}{g_{m4}}g_{m2}^2\right]v_1+\left(\frac{sC_3+g_{m5}}{g_{m4}}(g_{m2}+sC_2)-g_{m3}\right)(I_{N1}-I_{N2})$$
$$+\frac{sC_3+g_{m5}}{g_{m4}}g_{m2}(I_{N2}+I_{N4})-g_{m2}(I_{N3}+I_{N5})=0$$

(2.71)

It thus follows that v_1 can be expressed as

$$v_1 = \left[\frac{-\left(\frac{sC_3+g_{m5}}{g_{m4}}(g_{m2}+sC_2)-g_{m3}\right)I_{N1}+\left(sC_2\frac{sC_3+g_{m5}}{g_{m4}}-g_{m3}\right)I_{N2}-g_{m2}\left(\frac{sC_3+g_{m5}}{g_{m4}}I_{N4}-I_{N3}-I_{N5}\right)}{\left[\left(\frac{sC_3+g_{m5}}{g_{m4}}(g_{m2}+sC_2)-g_{m3}\right)(sC_1+g_{m1}+g_{m2})-\frac{sC_3+g_{m5}}{g_{m4}}g_{m2}^2\right]}\right]$$

(2.72)

To express the small-signal parameters in terms of design variables, the following relationships will be used. The small-signal parameters can be expressed either in terms of excess-bias voltages or device sizing ratios.

$$I_{D4Q} = MI_{D5Q} \tag{2.73}$$

$$I_{D1Q} = I_{DQ2} = MI_{D3Q} \tag{2.74}$$

$$P=V_{DD}\frac{(1+M)}{M}I_{D1Q} \tag{2.75}$$

$$g_{m1}=\frac{2I_{D1Q}}{V_{EB1}}=\frac{2PM}{V_{DD}V_{EB1}(1+M)} \tag{2.76}$$

$$\frac{g_{m5}}{g_{m4}}=\frac{I_{D5Q}}{I_{D4Q}}=\frac{1}{M} \tag{2.77}$$

$$\frac{g_{m2}}{g_{m1}}=\frac{V_{EB1}}{V_{EB2}}=\sqrt{\frac{W_2L_1}{W_1L_2}} \tag{2.78}$$

$$\frac{g_{m3}}{g_{m1}}=\frac{1}{M}\frac{V_{EB1}}{V_{EB3}}=\sqrt{\frac{W_3L_1}{MW_1L_3}} \tag{2.79}$$

It will now be assumed that the gate-source capacitance of the devices, C_{GS} , is the dominant component of C_1, C_2, and C_3. These gate-source capacitances can be expressed as

$$C_{GS}=\frac{2}{3}C_{OX}WL=\frac{2}{3}C_{OX}\frac{W}{L}L^2=\frac{4}{3}\frac{L^2}{\mu}\frac{I_{DQ}}{V_{EB}^2} \tag{2.80}$$

And, the small signal transconductance can be expressed as

$$g_m=\mu C_{OX}\frac{W}{L}V_{EB} \tag{2.81}$$

The transition frequency of each transistor can be expressed as

$$\omega_T=\frac{g_m}{C_{GS}}=\frac{3}{2}\frac{\mu V_{EB}}{L^2} \tag{2.82}$$

Then,

$$\frac{C_1}{g_{m1}} = \frac{\frac{2}{3}C_{OX}W_1L_1}{\mu_n C_{OX}\frac{W_1}{L_1}V_{EB1}} = \frac{2}{3}\frac{L_1^2}{\mu_n}\frac{1}{V_{EB1}} = \frac{1}{\omega_{T1}} \tag{2.83}$$

$$\frac{C_2}{g_{m1}} = \frac{\frac{4}{3}\frac{L_2^2}{\mu_n}\frac{I_{DQ2}}{V_{EB2}^2} + \frac{4}{3}\frac{L_3^2}{\mu_n}\frac{I_{DQ3}}{V_{EB3}^2}}{\frac{2I_{DQ1}}{V_{EB1}}} = \frac{\frac{2}{3}\frac{L_2^2}{\mu_n V_{EB2}}\frac{M}{V_{EB2}} + \frac{2}{3}\frac{L_3^2}{\mu_n V_{EB3}}\frac{1}{V_{EB3}}}{\frac{M}{V_{EB1}}} = \frac{1}{\omega_{T2}}\frac{V_{EB1}}{V_{EB2}} + \frac{1}{\omega_{T3}}\frac{V_{EB1}}{MV_{EB3}} \tag{2.84}$$

$$\frac{C_3}{g_{m4}} = \frac{\frac{4}{3}\frac{L_4^2}{\mu_p}\frac{I_{DQ4}}{V_{EB4}^2} + \frac{4}{3}\frac{L_5^2}{\mu_p}\frac{I_{DQ5}}{V_{EB5}^2}}{\frac{2I_{DQ4}}{V_{EB4}}} = \left(\frac{2}{3}\frac{L_4^2}{\mu_p V_{EB4}} + M\frac{2}{3}\frac{L_5^2}{\mu_p V_{EB5}}\right)\frac{1}{M} = \frac{1}{\omega_{T4}}\frac{1+M}{M} \tag{2.85}$$

Substituting into the expression for υ_1 in (2.72) yields

$$\upsilon_1 = \left[\frac{V_{DD}}{2P}\left(\frac{1+M}{M}\right)\right]V_{EB1}\left[\begin{array}{l} -\left[\left(\frac{s}{\omega_{T4}}(1+M)+1\right)\left(s\left(\frac{1}{\omega_{T2}}+\frac{1}{\omega_{T3}}\frac{V_{EB2}}{MV_{EB3}}\right)+1\right)-\frac{V_{EB2}}{V_{EB3}}\right]I_{N1} \\ +\left[s\left(\frac{1}{\omega_{T2}}+\frac{1}{\omega_{T3}}\frac{V_{EB2}}{MV_{EB3}}\right)\left(\frac{s}{\omega_{T4}}(1+M)+1\right)-\frac{V_{EB2}}{V_{EB3}}\right]I_{N2}-\left[\frac{s}{\omega_{T4}}(1+M)+1\right]I_{N4}+MI_{N3}+MI_{N5} \\ \hline \left[\left(\frac{s}{\omega_{T4}}(1+M)+1\right)\left(s\left(\frac{1}{\omega_{T2}}+\frac{1}{\omega_{T3}}\frac{V_{EB2}}{MV_{EB3}}\right)+1\right)-\frac{V_{EB2}}{V_{EB3}}\right]\left[\frac{s}{\omega_{T1}}+1+\frac{V_{EB1}}{V_{EB2}}\right]-\left(\frac{s}{\omega_{T4}}(1+M)+1\right)\left(\frac{V_{EB1}}{V_{EB2}}\right) \end{array}\right] \tag{2.86}$$

Following the notation used in equation (2.57)(2.49), the term multiplying each noise current is the transfer function from that current source to the output υ_1. Denoting the transfer function from the k^{th} noise source to υ_1 as $T_{k1}(s)$, it follows that these transfer functions can be expressed as:

$$T_{11}(s)=\left[\frac{V_{DD}}{2P}\left(\frac{1+M}{M}\right)\right]V_{EB1}\frac{\left[\frac{V_{EB2}}{V_{EB3}}-\left(\frac{s}{\omega_{T4}}(1+M)+1\right)\left(s\left(\frac{1}{\omega_{T2}}+\frac{1}{\omega_{T3}}\frac{V_{EB2}}{MV_{EB3}}\right)+1\right)\right]}{\left[\left(\frac{s}{\omega_{T4}}(1+M)+1\right)\left(s\left(\frac{1}{\omega_{T2}}+\frac{1}{\omega_{T3}}\frac{V_{EB2}}{MV_{EB3}}\right)+1\right)-\frac{V_{EB2}}{V_{EB3}}\right]\left[\frac{s}{\omega_{T1}}+1+\frac{V_{EB1}}{V_{EB2}}\right]-\left(\frac{s}{\omega_{T4}}(1+M)+1\right)\left(\frac{V_{EB1}}{V_{EB2}}\right)}$$

(2.87)

$$T_{21}(s)=\left[\frac{V_{DD}}{2P}\left(\frac{1+M}{M}\right)\right]V_{EB1}\frac{\left[s\left(\frac{1}{\omega_{T2}}+\frac{1}{\omega_{T3}}\frac{V_{EB2}}{MV_{EB3}}\right)\left(\frac{s}{\omega_{T4}}(1+M)+1\right)-\frac{V_{EB2}}{V_{EB3}}\right]}{\left[\left(\frac{s}{\omega_{T4}}(1+M)+1\right)\left(s\left(\frac{1}{\omega_{T2}}+\frac{1}{\omega_{T3}}\frac{V_{EB2}}{MV_{EB3}}\right)+1\right)-\frac{V_{EB2}}{V_{EB3}}\right]\left[\frac{s}{\omega_{T1}}+1+\frac{V_{EB1}}{V_{EB2}}\right]-\left(\frac{s}{\omega_{T4}}(1+M)+1\right)\left(\frac{V_{EB1}}{V_{EB2}}\right)}$$

(2.88)

$$T_{31}(s)=\left[\frac{V_{DD}}{2P}\left(\frac{1+M}{M}\right)\right]V_{EB1}\frac{M}{\left[\left(\frac{s}{\omega_{T4}}(1+M)+1\right)\left(s\left(\frac{1}{\omega_{T2}}+\frac{1}{\omega_{T3}}\frac{V_{EB2}}{MV_{EB3}}\right)+1\right)-\frac{V_{EB2}}{V_{EB3}}\right]\left[\frac{s}{\omega_{T1}}+1+\frac{V_{EB1}}{V_{EB2}}\right]-\left(\frac{s}{\omega_{T4}}(1+M)+1\right)\left(\frac{V_{EB1}}{V_{EB2}}\right)}$$

(2.89)

$$T_{41}(s)=\left[\frac{V_{DD}}{2P}\left(\frac{1+M}{M}\right)\right]V_{EB1}\frac{-\left[\frac{s}{\omega_{T4}}(1+M)+1\right]}{\left[\left(\frac{s}{\omega_{T4}}(1+M)+1\right)\left(s\left(\frac{1}{\omega_{T2}}+\frac{1}{\omega_{T3}}\frac{V_{EB2}}{MV_{EB3}}\right)+1\right)-\frac{V_{EB2}}{V_{EB3}}\right]\left[\frac{s}{\omega_{T1}}+1+\frac{V_{EB1}}{V_{EB2}}\right]-\left(\frac{s}{\omega_{T4}}(1+M)+1\right)\left(\frac{V_{EB1}}{V_{EB2}}\right)}$$

(2.90)

$$T_{51}(s)=\left[\frac{V_{DD}}{2P}\left(\frac{1+M}{M}\right)\right]V_{EB1}\frac{M}{\left[\left(\frac{s}{\omega_{T4}}(1+M)+1\right)\left(s\left(\frac{1}{\omega_{T2}}+\frac{1}{\omega_{T3}}\frac{V_{EB2}}{MV_{EB3}}\right)+1\right)-\frac{V_{EB2}}{V_{EB3}}\right]\left[\frac{s}{\omega_{T1}}+1+\frac{V_{EB1}}{V_{EB2}}\right]-\left(\frac{s}{\omega_{T4}}(1+M)+1\right)\left(\frac{V_{EB1}}{V_{EB2}}\right)}$$

(2.91)

It can be observed that all transfer functions have a low-pass characteristic. Though these transfer functions all have the same denominator polynomial, evaluation of thee transfer

functions depends upon three values of ω_T which may differ from one design to the next. In an attempt to simplify the transfer functions a bit, a new approximate transfer function $\hat{T}_{k1}(s)$ is defined for each of the transfer functions $T_{k1}(s)$ by setting $\omega_{T1}=\omega_{T2}=\omega_{T3}=\omega_{T4}=\omega_T$ in each of these transfer functions. If the ω_{Tk} values are close to each other and if ω_T is selected so that it is close to these values as well, then the approximate transfer functions $\hat{T}_{k1}(s)$ will not differ significantly from $T_{k1}(s)$. If there are appreciable differences in the ω_T values, then the approximate transfer functions will differ somewhat from the actual transfer functions. In the next section, the value of ω_T will be set to be the maximum of $\{\omega_{T1},\omega_{T2},\omega_{T3},\omega_{T4}\}$. The rationale of this selection of ω_T is that the flicker noise will be modestly over estimated. It thus follows that

$$\hat{T}_{11}(s)=\frac{-\left[\frac{V_{DD}}{2P}\left(\frac{1+M}{M}\right)V_{EB1}\right]\left[\frac{s^2}{\omega_T^2}(1+M)\left(1+\frac{V_{EB2}}{MV_{EB3}}\right)+\frac{s}{\omega_T}\left(2+M+\frac{V_{EB2}}{MV_{EB3}}\right)+1-\frac{V_{EB2}}{V_{EB3}}\right]}{\left[\begin{array}{l}\frac{s^3}{\omega_T^3}(1+M)\left(1+\frac{V_{EB2}}{MV_{EB3}}\right)+\frac{s^2}{\omega_T^2}\left(3+2M+\frac{(1+M)V_{EB1}+(2+M)V_{EB2}}{MV_{EB3}}+(1+M)\frac{V_{EB1}}{V_{EB2}}\right)\\+\frac{s}{\omega_T}\left(2+\frac{V_{EB1}+(1-M)V_{EB2}}{MV_{EB3}}+(2+M)\frac{V_{EB1}}{V_{EB2}}\right)+\left(1-\frac{V_{EB1}+V_{EB2}}{V_{EB3}}\right)\end{array}\right]} \tag{2.92}$$

$$\hat{T}_{21}(s)=\frac{\left[\frac{V_{DD}}{2P}\left(\frac{1+M}{M}\right)V_{EB1}\right]\left[\frac{s^2}{\omega_T^2}(1+M)\left(1+\frac{V_{EB2}}{MV_{EB3}}\right)+\frac{s}{\omega_T}\left(1+\frac{V_{EB2}}{MV_{EB3}}\right)-\frac{V_{EB2}}{V_{EB3}}\right]}{\left[\begin{array}{l}\frac{s^3}{\omega_T^3}(1+M)\left(1+\frac{V_{EB2}}{MV_{EB3}}\right)+\frac{s^2}{\omega_T^2}\left(3+2M+\frac{(1+M)V_{EB1}+(2+M)V_{EB2}}{MV_{EB3}}+(1+M)\frac{V_{EB1}}{V_{EB2}}\right)\\+\frac{s}{\omega_T}\left(2+\frac{V_{EB1}+(1-M)V_{EB2}}{MV_{EB3}}+(2+M)\frac{V_{EB1}}{V_{EB2}}\right)+\left(1-\frac{V_{EB1}+V_{EB2}}{V_{EB3}}\right)\end{array}\right]} \tag{2.93}$$

$$\hat{T}_{31}(s)=\frac{\left[\frac{V_{DD}}{2P}(1+M)V_{EB1}\right]}{\left[\begin{array}{l}\frac{s^3}{\omega_T^3}(1+M)\left(1+\frac{V_{EB2}}{MV_{EB3}}\right)+\frac{s^2}{\omega_T^2}\left(3+2M+\frac{(1+M)V_{EB1}+(2+M)V_{EB2}}{MV_{EB3}}+(1+M)\frac{V_{EB1}}{V_{EB2}}\right)\\+\frac{s}{\omega_T}\left(2+\frac{V_{EB1}+(1-M)V_{EB2}}{MV_{EB3}}+(2+M)\frac{V_{EB1}}{V_{EB2}}\right)+\left(1-\frac{V_{EB1}+V_{EB2}}{V_{EB3}}\right)\end{array}\right]} \tag{2.94}$$

$$\hat{T}_{41}(s)=\frac{-\left[\frac{V_{DD}}{2P}\left(\frac{1+M}{M}\right)V_{EB1}\right]\left[\frac{s}{\omega_T}(1+M)+1\right]}{\left[\begin{array}{l}\frac{s^3}{\omega_T^3}(1+M)\left(1+\frac{V_{EB2}}{MV_{EB3}}\right)+\frac{s^2}{\omega_T^2}\left(3+2M+\frac{(1+M)V_{EB1}+(2+M)V_{EB2}}{MV_{EB3}}+(1+M)\frac{V_{EB1}}{V_{EB2}}\right)\\+\frac{s}{\omega_T}\left(2+\frac{V_{EB1}+(1-M)V_{EB2}}{MV_{EB3}}+(2+M)\frac{V_{EB1}}{V_{EB2}}\right)+\left(1-\frac{V_{EB1}+V_{EB2}}{V_{EB3}}\right)\end{array}\right]} \tag{2.95}$$

$$\hat{T}_{51}(s)=\frac{\left[\frac{V_{DD}}{2P}(1+M)V_{EB1}\right]}{\left[\begin{array}{l}\frac{s^3}{\omega_T^3}(1+M)\left(1+\frac{V_{EB2}}{MV_{EB3}}\right)+\frac{s^2}{\omega_T^2}\left(3+2M+\frac{(1+M)V_{EB1}+(2+M)V_{EB2}}{MV_{EB3}}+(1+M)\frac{V_{EB1}}{V_{EB2}}\right)\\+\frac{s}{\omega_T}\left(2+\frac{V_{EB1}+(1-M)V_{EB2}}{MV_{EB3}}+(2+M)\frac{V_{EB1}}{V_{EB2}}\right)+\left(1-\frac{V_{EB1}+V_{EB2}}{V_{EB3}}\right)\end{array}\right]} \tag{2.96}$$

The complex value of these transfer functions can be obtained by substituting $s=j\omega$.

$$\hat{T}_{11}(j\omega)=\frac{-\left[\frac{V_{DD}}{2P}\left(\frac{1+M}{M}\right)\right]\left[1-\frac{V_{EB2}}{V_{EB3}}-\frac{\omega}{\omega_T^2}\left(1+M+\frac{(1+M)V_{EB2}}{MV_{EB3}}\right)+j\frac{\omega}{\omega_T}\left(2+M+\frac{V_{EB2}}{MV_{EB3}}\right)\right]V_{EB1}}{\left[\begin{array}{l}\left(1-\frac{V_{EB1}+V_{EB2}}{V_{EB3}}\right)-\frac{\omega^2}{\omega_T^2}\left(3+2M+\frac{(1+M)V_{EB1}+(2+M)V_{EB2}}{MV_{EB3}}+\frac{(1+M)V_{EB1}}{V_{EB2}}\right)\\+j\left[\frac{\omega}{\omega_T}\left(2+\frac{V_{EB1}+(1-M)V_{EB2}}{MV_{EB3}}+(2+M)\frac{V_{EB1}}{V_{EB2}}\right)-\frac{\omega^3}{\omega_T^3}\left(1+M+\frac{(1+M)V_{EB2}}{MV_{EB3}}\right)\right]\end{array}\right]} \tag{2.97}$$

$$\hat{T}_{21}(j\omega)=\frac{\left[\frac{V_{DD}}{2P}\left(\frac{1+M}{M}\right)\right]\left[\frac{\omega^2}{\omega_T^2}\left(1+M+\frac{(1+M)V_{EB2}}{MV_{EB3}}\right)-\frac{V_{EB2}}{V_{EB3}}+j\frac{\omega}{\omega_T}\left(1+\frac{V_{EB2}}{MV_{EB3}}\right)\right]V_{EB1}}{\left[\begin{array}{l}\left(1-\frac{V_{EB1}+V_{EB2}}{V_{EB3}}\right)-\frac{\omega^2}{\omega_T^2}\left(3+2M+\frac{(1+M)V_{EB1}+(2+M)V_{EB2}}{MV_{EB3}}+\frac{(1+M)V_{EB1}}{V_{EB2}}\right)\\+j\left[\frac{\omega}{\omega_T}\left(2+\frac{V_{EB1}+(1-M)V_{EB2}}{MV_{EB3}}+(2+M)\frac{V_{EB1}}{V_{EB2}}\right)-\frac{\omega^3}{\omega_T^3}\left(1+M+\frac{(1+M)V_{EB2}}{MV_{EB3}}\right)\right]\end{array}\right]} \tag{2.98}$$

$$\hat{T}_{31}(j\omega)=\frac{\left[\frac{V_{DD}}{2P}(1+M)\right]V_{EB1}}{\left[\begin{array}{l}\left(1-\frac{V_{EB1}+V_{EB2}}{V_{EB3}}\right)-\frac{\omega^2}{\omega_T^2}\left(3+2M+\frac{(1+M)V_{EB1}+(2+M)V_{EB2}}{MV_{EB3}}+\frac{(1+M)V_{EB1}}{V_{EB2}}\right)\\+j\left[\frac{\omega}{\omega_T}\left(2+\frac{V_{EB1}+(1-M)V_{EB2}}{MV_{EB3}}+(2+M)\frac{V_{EB1}}{V_{EB2}}\right)-\frac{\omega^3}{\omega_T^3}\left(1+M+\frac{(1+M)V_{EB2}}{MV_{EB3}}\right)\right]\end{array}\right]} \tag{2.99}$$

$$\hat{T}_{41}(j\omega)=\frac{-\left[\frac{V_{DD}}{2P}\left(\frac{1+M}{M}\right)\right]\left[1+j\frac{\omega}{\omega_T}(1+M)\right]V_{EB1}}{\left[\left(1-\frac{V_{EB1}+V_{EB2}}{V_{EB3}}\right)-\frac{\omega^2}{\omega_T^2}\left(3+2M+\frac{(1+M)V_{EB1}+(2+M)V_{EB2}}{MV_{EB3}}+\frac{(1+M)V_{EB1}}{V_{EB2}}\right)\right]+j\left[\frac{\omega}{\omega_T}\left(2+\frac{V_{EB1}+(1-M)V_{EB2}}{MV_{EB3}}+(2+M)\frac{V_{EB1}}{V_{EB2}}\right)-\frac{\omega^3}{\omega_T^3}\left(1+M+\frac{(1+M)V_{EB2}}{MV_{EB3}}\right)\right]} \quad (2.100)$$

$$\hat{T}_{51}(j\omega)=\frac{\left[\frac{V_{DD}}{2P}(1+M)\right]V_{EB1}}{\left[\left(1-\frac{V_{EB1}+V_{EB2}}{V_{EB3}}\right)-\frac{\omega^2}{\omega_T^2}\left(3+2M+\frac{(1+M)V_{EB1}+(2+M)V_{EB2}}{MV_{EB3}}+\frac{(1+M)V_{EB1}}{V_{EB2}}\right)\right]+j\left[\frac{\omega}{\omega_T}\left(2+\frac{V_{EB1}+(1-M)V_{EB2}}{MV_{EB3}}+(2+M)\frac{V_{EB1}}{V_{EB2}}\right)-\frac{\omega^3}{\omega_T^3}\left(1+M+\frac{(1+M)V_{EB2}}{MV_{EB3}}\right)\right]} \quad (2.101)$$

Assuming all noise sources are independent (no correlation with each other), it now follows from (2.57) that the spectral density of the output voltage is given by the expression.

$$S_{OUT1}=\left|T_1(j\omega)\right|^2 S_1+\left|T_2(j\omega)\right|^2 S_2+\left|T_3(j\omega)\right|^2 S_3+\left|T_4(j\omega)\right|^2 S_4+\left|T_5(j\omega)\right|^2 S_5 \quad (2.102)$$

$$S_n=\frac{8}{3}kTg_m+\frac{K_F I_{ds}^{AF}}{C_{ox}L_{eff}^2 f^{EF}} \quad (2.103)$$

And, the spectral density at the output can be approximated by the expression

$$\hat{S}_{OUT1}=\left|\hat{T}_{11}(j\omega)\right|^2 S_1+\left|\hat{T}_{21}(j\omega)\right|^2 S_2+\left|\hat{T}_{31}(j\omega)\right|^2 S_3+\left|\hat{T}_{41}(j\omega)\right|^2 S_4+\left|\hat{T}_{51}(j\omega)\right|^2 S_5 \quad (2.104)$$

The product of the transfer function magnitude squared and the corresponding noise spectral density represents the output-referred contribution due to each of the noise sources. For notational convenience, the output referred contribution to the spectral density due to each

noise source will be denoted as S_{k1} and the approximate spectral densities as $\hat{S}_{k1}$. With this notation, it follows from (2.57) that the output spectral density is given by

$$S_{OUT1} = \sum_{k=1}^{5} S_{k1} \tag{2.105}$$

and the approximate spectral density is given by

$$\hat{S}_{OUT1} = \sum_{k=1}^{5} \hat{S}_{k1} \tag{2.106}$$

The approximate terms $\hat{S}_{11}, \hat{S}_{21}, \hat{S}_{31}, \hat{S}_{41}, \hat{S}_{51}$ are given by

$$\hat{S}_{11} = \left|\hat{T}_{11}(j\omega)\right|^2 S_1 = \left[\frac{\left[\frac{V_{DD}}{2P}\left(\frac{1+M}{M}\right)V_{EB1}\right]^2\left[\left(1-\frac{V_{EB2}}{V_{EB3}}-\frac{\omega}{\omega_T^2}\left(1+M+\frac{(1+M)V_{EB2}}{MV_{EB3}}\right)\right)^2+\left(\frac{\omega}{\omega_T}\left(2+M+\frac{V_{EB2}}{MV_{EB3}}\right)\right)^2\right]}{\left[\left(1-\frac{V_{EB1}+V_{EB2}}{V_{EB3}}\right)-\frac{\omega^2}{\omega_T^2}\left(3+2M+\frac{(1+M)V_{EB1}+(2+M)V_{EB2}}{MV_{EB3}}+\frac{(1+M)V_{EB1}}{V_{EB2}}\right)\right]^2 + \left[\frac{\omega}{\omega_T}\left(2+\frac{V_{EB1}+(1-M)V_{EB2}}{MV_{EB3}}+(2+M)\frac{V_{EB1}}{V_{EB2}}\right)-\frac{\omega^3}{\omega_T^3}\left(1+M+\frac{(1+M)V_{EB2}}{MV_{EB3}}\right)\right]^2}\right] S_1 \tag{2.107}$$

$$\hat{S}_{21} = \left|\hat{T}_{21}(j\omega)\right|^2 S_2 = \left[\frac{\left[\frac{V_{DD}}{2P}\left(\frac{1+M}{M}\right)V_{EB1}\right]^2\left[\left(\frac{\omega^2}{\omega_T^2}\left(1+M+\frac{(1+M)V_{EB2}}{MV_{EB3}}\right)-\frac{V_{EB2}}{V_{EB3}}\right)^2+\left(\frac{\omega}{\omega_T}\left(1+\frac{V_{EB2}}{MV_{EB3}}\right)\right)^2\right]}{\left[\left(1-\frac{V_{EB1}+V_{EB2}}{V_{EB3}}\right)-\frac{\omega^2}{\omega_T^2}\left(3+2M+\frac{(1+M)V_{EB1}+(2+M)V_{EB2}}{MV_{EB3}}+\frac{(1+M)V_{EB1}}{V_{EB2}}\right)\right]^2 + \left[\frac{\omega}{\omega_T}\left(2+\frac{V_{EB1}+(1-M)V_{EB2}}{MV_{EB3}}+(2+M)\frac{V_{EB1}}{V_{EB2}}\right)-\frac{\omega^3}{\omega_T^3}\left(1+M+\frac{(1+M)V_{EB2}}{MV_{EB3}}\right)\right]^2}\right] S_2 \tag{2.108}$$

$$\hat{S}_{31}=\left|\hat{T}_{31}(j\omega)\right|^2 S_3=\left[\frac{\left[\frac{V_{DD}}{2P}(1+M)V_{EB1}\right]^2}{\left[\left(1-\frac{V_{EB1}+V_{EB2}}{V_{EB3}}\right)-\frac{\omega^2}{\omega_T^2}\left(3+2M+\frac{(1+M)V_{EB1}+(2+M)V_{EB2}}{MV_{EB3}}+\frac{(1+M)V_{EB1}}{V_{EB2}}\right)\right]^2+\left[\frac{\omega}{\omega_T}\left(2+\frac{V_{EB1}+(1-M)V_{EB2}}{MV_{EB3}}+(2+M)\frac{V_{EB1}}{V_{EB2}}\right)-\frac{\omega^3}{\omega_T^3}\left(1+M+\frac{(1+M)V_{EB2}}{MV_{EB3}}\right)\right]^2}\right]S_3 \tag{2.109}$$

$$\hat{S}_{41}=\left|\hat{T}_{41}(j\omega)\right|^2 S_4=\left[\frac{\left[\frac{V_{DD}}{2P}\left(\frac{1+M}{M}\right)V_{EB1}\right]^2\left[1+\left(\frac{\omega}{\omega_T}(1+M)\right)^2\right]}{\left[\left(1-\frac{V_{EB1}+V_{EB2}}{V_{EB3}}\right)-\frac{\omega^2}{\omega_T^2}\left(3+2M+\frac{(1+M)V_{EB1}+(2+M)V_{EB2}}{MV_{EB3}}+\frac{(1+M)V_{EB1}}{V_{EB2}}\right)\right]^2+\left[\frac{\omega}{\omega_T}\left(2+\frac{V_{EB1}+(1-M)V_{EB2}}{MV_{EB3}}+(2+M)\frac{V_{EB1}}{V_{EB2}}\right)-\frac{\omega^3}{\omega_T^3}\left(1+M+\frac{(1+M)V_{EB2}}{MV_{EB3}}\right)\right]^2}\right]S_4 \tag{2.110}$$

$$\hat{S}_{51}=\left|\hat{T}_{51}(j\omega)\right|^2 S_5=\left[\frac{\left[\frac{V_{DD}}{2P}(1+M)V_{EB1}\right]^2}{\left[\left(1-\frac{V_{EB1}+V_{EB2}}{V_{EB3}}\right)-\frac{\omega^2}{\omega_T^2}\left(3+2M+\frac{(1+M)V_{EB1}+(2+M)V_{EB2}}{MV_{EB3}}+\frac{(1+M)V_{EB1}}{V_{EB2}}\right)\right]^2+\left[\frac{\omega}{\omega_T}\left(2+\frac{V_{EB1}+(1-M)V_{EB2}}{MV_{EB3}}+(2+M)\frac{V_{EB1}}{V_{EB2}}\right)-\frac{\omega^3}{\omega_T^3}\left(1+M+\frac{(1+M)V_{EB2}}{MV_{EB3}}\right)\right]^2}\right]S_5 \tag{2.111}$$

Up to this point, the spectral densities have been expressed in terms of the excess bias voltages, P, ω_T, and M. For analytical purposes, it may also be useful to express the spectral densities in terms of the design variables. The relationship between the excess bias voltages and the W/L ratios are:

$$\frac{V_{EB1}}{V_{EB2}}=\sqrt{\frac{W_2L_1}{W_1L_2}} \tag{2.112}$$

$$\frac{V_{EB1}}{V_{EB3}} = \sqrt{\frac{MW_3L_1}{W_1L_3}} \tag{2.113}$$

$$\frac{V_{EB2}}{V_{EB3}} = \sqrt{\frac{MW_3L_2}{W_2L_3}} \tag{2.114}$$

$$\frac{V_{EB4}}{V_{EB3}} = \sqrt{\frac{\mu_n W_3 L_4}{\mu_p M W_4 L_3}} \tag{2.115}$$

Thus, in terms of the W/L ratios, M, and P, the spectral densities of (2.107) – (2.111) can be expressed equivalently as;

$$\hat{S}_{11} = \left[\frac{\left(\frac{L_1}{2\mu_n C_{ox} W_1}\right)\left(\frac{V_{DD}}{P}\frac{1+M}{M}\right)\left[\left(1-\sqrt{\frac{MW_3L_2}{W_2L_3}}-\frac{\omega^2}{\omega_T^2}\left(1+M+(1+M)\sqrt{\frac{W_3L_2}{MW_2L_3}}\right)\right)^2+\left(\frac{\omega}{\omega_T}\left(2+M+\sqrt{\frac{W_3L_2}{MW_2L_3}}\right)\right)^2\right]}{\left[\left(1-\sqrt{\frac{MW_3}{L_3}}\left(\sqrt{\frac{L_1}{W_1}}+\sqrt{\frac{L_2}{W_2}}\right)\right)-\frac{\omega^2}{\omega_T^2}\left((1+M)\left(1+\sqrt{\frac{W_3L_1}{MW_1L_3}}+\sqrt{\frac{W_2L_1}{W_1L_2}}\right)+(2+M)\left(1+\sqrt{\frac{W_3L_2}{MW_2L_3}}\right)\right)\right]^2} \right. \\ \left. +\left[\frac{\omega}{\omega_T}\left(2+\sqrt{\frac{W_3L_1}{MW_1L_3}}+(1-M)\sqrt{\frac{W_3L_2}{MW_2L_3}}+(2+M)\sqrt{\frac{W_2L_1}{W_1L_2}}\right)-\frac{\omega^3}{\omega_T^3}\left((1+M)\left(1+\sqrt{\frac{W_3L_2}{MW_2L_3}}\right)\right)\right]^2 \right] S_1 \tag{2.116}$$

$$\hat{S}_{21} = \left[\frac{\left(\frac{L_1}{2\mu_n C_{ox} W_1}\right)\left(\frac{V_{DD}}{P}\frac{1+M}{M}\right)\left[\left(\frac{\omega^2}{\omega_T^2}\left(1+M+(1+M)\sqrt{\frac{W_3L_2}{MW_2L_3}}\right)-\sqrt{\frac{MW_3L_2}{W_2L_3}}\right)^2+\left(\frac{\omega}{\omega_T}\left(1+\sqrt{\frac{W_3L_2}{MW_2L_3}}\right)\right)^2\right]}{\left[\left(1-\sqrt{\frac{MW_3}{L_3}}\left(\sqrt{\frac{L_1}{W_1}}+\sqrt{\frac{L_2}{W_2}}\right)\right)-\frac{\omega^2}{\omega_T^2}\left((1+M)\left(1+\sqrt{\frac{W_3L_1}{MW_1L_3}}+\sqrt{\frac{W_2L_1}{W_1L_2}}\right)+(2+M)\left(1+\sqrt{\frac{W_3L_2}{MW_2L_3}}\right)\right)\right]^2} \right. \\ \left. +\left[\frac{\omega}{\omega_T}\left(2+\sqrt{\frac{W_3L_1}{MW_1L_3}}+(1-M)\sqrt{\frac{W_3L_2}{MW_2L_3}}+(2+M)\sqrt{\frac{W_2L_1}{W_1L_2}}\right)-\frac{\omega^3}{\omega_T^3}\left((1+M)\left(1+\sqrt{\frac{W_3L_2}{MW_2L_3}}\right)\right)\right]^2 \right] S_2 \tag{2.117}$$

$$\hat{S}_{31}=\left[\frac{\left(\frac{L_1}{2\mu_n C_{ox}W_1}\right)\left(\frac{V_{DD}}{P}\frac{1+M}{M}\right)}{\left[\left(1-\sqrt{\frac{MW_3}{L_3}}\left(\sqrt{\frac{L_1}{W_1}}+\sqrt{\frac{L_2}{W_2}}\right)\right)-\frac{\omega^2}{\omega_T^2}\left((1+M)\left(1+\sqrt{\frac{W_3L_1}{MW_1L_3}}+\sqrt{\frac{W_2L_1}{W_1L_2}}\right)+(2+M)\left(1+\sqrt{\frac{W_3L_2}{MW_2L_3}}\right)\right)\right]^2}\right.$$
$$\left.+\left[\frac{\omega}{\omega_T}\left(2+\sqrt{\frac{W_3L_1}{MW_1L_3}}+(1-M)\sqrt{\frac{W_3L_2}{MW_2L_3}}+(2+M)\sqrt{\frac{W_2L_1}{W_1L_2}}\right)-\frac{\omega^3}{\omega_T^3}\left((1+M)\left(1+\sqrt{\frac{W_3L_2}{MW_2L_3}}\right)\right)\right]^2\right] S_3 \quad (2.118)$$

$$\hat{S}_{41}=\left[\frac{\left(\frac{L_1}{2\mu_n C_{ox}W_1}\right)\left(\frac{V_{DD}}{P}\frac{1+M}{M}\right)\left[1+\left(\frac{\omega}{\omega_T}(1+M)\right)^2\right]}{\left[\left(1-\sqrt{\frac{MW_3}{L_3}}\left(\sqrt{\frac{L_1}{W_1}}+\sqrt{\frac{L_2}{W_2}}\right)\right)-\frac{\omega^2}{\omega_T^2}\left((1+M)\left(1+\sqrt{\frac{W_3L_1}{MW_1L_3}}+\sqrt{\frac{W_2L_1}{W_1L_2}}\right)+(2+M)\left(1+\sqrt{\frac{W_3L_2}{MW_2L_3}}\right)\right)\right]^2}\right.$$
$$\left.+\left[\frac{\omega}{\omega_T}\left(2+\sqrt{\frac{W_3L_1}{MW_1L_3}}+(1-M)\sqrt{\frac{W_3L_2}{MW_2L_3}}+(2+M)\sqrt{\frac{W_2L_1}{W_1L_2}}\right)-\frac{\omega^3}{\omega_T^3}\left((1+M)\left(1+\sqrt{\frac{W_3L_2}{MW_2L_3}}\right)\right)\right]^2\right] S_4 \quad (2.119)$$

$$\hat{S}_{51}=\left[\frac{\left(\frac{L_1}{2\mu_n C_{ox}W_1}\right)\left(\frac{V_{DD}}{P}\frac{1+M}{M}\right)}{\left[\left(1-\sqrt{\frac{MW_3}{L_3}}\left(\sqrt{\frac{L_1}{W_1}}+\sqrt{\frac{L_2}{W_2}}\right)\right)-\frac{\omega^2}{\omega_T^2}\left((1+M)\left(1+\sqrt{\frac{W_3L_1}{MW_1L_3}}+\sqrt{\frac{W_2L_1}{W_1L_2}}\right)+(2+M)\left(1+\sqrt{\frac{W_3L_2}{MW_2L_3}}\right)\right)\right]^2}\right.$$
$$\left.+\left[\frac{\omega}{\omega_T}\left(2+\sqrt{\frac{W_3L_1}{MW_1L_3}}+(1-M)\sqrt{\frac{W_3L_2}{MW_2L_3}}+(2+M)\sqrt{\frac{W_2L_1}{W_1L_2}}\right)-\frac{\omega^3}{\omega_T^3}\left((1+M)\left(1+\sqrt{\frac{W_3L_2}{MW_2L_3}}\right)\right)\right]^2\right] S_5 \quad (2.120)$$

These expressions are then used to predict the noise performance of the circuit by evaluating the design parameters. We will now bring to closure this noise analysis in the context of the Reverse Widlar temperature sensor. From (2.57), the spectral density of the output can be expressed as

$$S_{OUT1}=\sum_{i=1}^{5}\left|T_i(j\omega)\right|^2 S_i \quad (2.121)$$

and the approximate spectral density at the output is given by

$$\hat{S}_{OUT1} = \sum_{i=1}^{5} \hat{S}_{i1} \tag{2.122}$$

From (2.58), (2.64), and (2.65), the RMS noise temperature is given by

$$T_{[f_{START},\infty]} = \frac{1}{\gamma} \sqrt{\int_{f_{START}}^{\infty} \left[\sum_{i=1}^{5} \left(\left| T_{i1}(j\omega) \right|^2 S_i \right) \right] df} \tag{2.123}$$

From an extension of (2.54) and (2.55), the flicker and white RMS noise temperatures can be approximately expressed as

$$T_{RMS-Flicker[f_{START},\infty]} \simeq \frac{1}{\gamma} \sqrt{\int_{f_{START}}^{f_{NCH}} \left[\sum_{i=1}^{5} \left(\left| T_{i1}(j\omega) \right|^2 \frac{K_{Fi} I_{Di}^{AFi}}{C_{OX} L_{effi}^2 f^{EFFi}} \right) \right] df} \tag{2.124}$$

$$T_{RMS-Thermal[f_{START},\infty]} \simeq \frac{1}{\gamma} \sqrt{\int_{f_{START}}^{f_{NCL}} \left[\sum_{i=1}^{5} \left(\left| T_{i1}(j\omega) \right|^2 \frac{8}{3} k T g_{mi} \right) \right] df} \tag{2.125}$$

where f_{NCH} is the highest of the noise corner frequencies and where f_{NCL} is the lowest of the noise corner frequencies.

Since the pole frequencies of the transfer functions are typically somewhat higher than the noise corner frequencies, the lowpass transfer functions do not differ much from their dc values so the flicker noise temperature can be expressed as

$$T_{RMS-Flicker[f_{START},\infty]} \simeq \frac{1}{\gamma} \sqrt{\int_{f_{START}}^{f_{NCH}} \left[\sum_{i=1}^{5} \left(\left| T_{i1}(j0) \right|^2 \frac{K_{Fi} I_{Di}^{AFi}}{C_{OX} L_{effi}^2 f^{EFFi}} \right) \right] df} \tag{2.126}$$

Finally, the expressions in (2.123) – (2.126) can be simplified somewhat by replacing the transfer functions $T_{k1}(j\omega)$ with the approximate transfer functions $\hat{T}_{k1}(j\omega)$.

ANALYTICAL AND SIMULATION RESULTS OF N-TYPE REVERSE WIDLAR TEMPERATURE SENSOR

The N-type 5T temperature sensor from [**17**] is used for the noise analysis. The following table shows the device sizes.

Table 2-3: Transistors size for P-type reverse Widlar temperature sensor

Transistor	M_1	M_2	M_3	M_4	M_5
Size (µm)	$\frac{W_1}{L_1}=\frac{2\times 7}{0.4}$	$\frac{W_2}{L_2}=\frac{2\times 5}{0.4}$	$\frac{W_3}{L_3}=\frac{0.3}{0.9}$	$\frac{W_4}{L_4}=\frac{4.5}{0.9}$	$\frac{W_5}{L_5}=\frac{4.5}{0.9}$

The analytical noise expression for the spectral density at the output has been evaluated and compared with the simulation output from Cadence SPECTRE. These comparisons are shown in Figure 2-22. In the SPECTRE simulation, the key noise model parameters were $KF_n = 5.9\times 10^{-28}\,V^2F$, $KF_p = 7.8\times 10^{-26}\,V^2F$, $AF_n = 1.0$, $A_{Fp} = 1.4$, $EFF_n = 0.8$, and $EFF_p = 1.1$. In the analytical analysis, the transfer function approximation was used where $\omega_T = \max\{\omega_{T1},\omega_{T2},\omega_{T3},\omega_{T4}\}$ where $\omega_T = 2\pi f_T$. In this design, the values for these parameters were $f_{T1} = 484\,MHz, f_{T2} = 486\,MHz, f_{T3} = 240\,MHz\ and\ f_{T4} = 1.81GHz$.

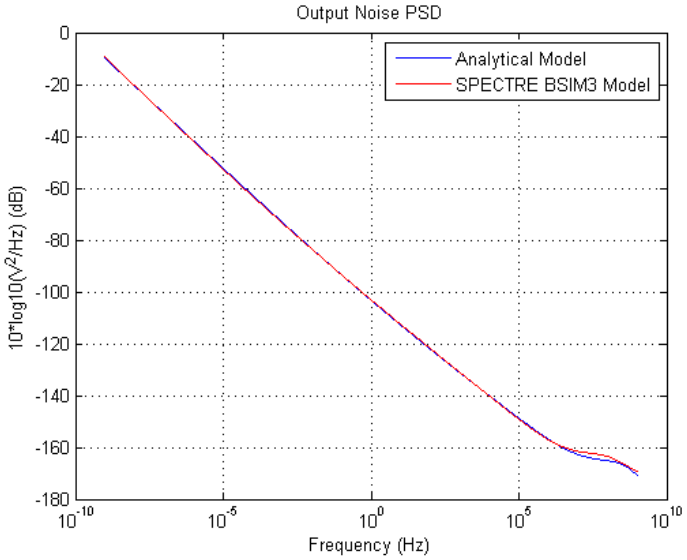


Figure 2-22: Output noise power spectral density for N-type 5T temperature sensor

From this analysis, it can be observed that the analytical approximations agree closely with the simulation results throughout the flicker noise region. There is a modest difference in the thermal noise region but in this structure, the noise performance is dominated by the flicker noise.

The time-domain RMS noise temperature was obtained for different operating times, T_{OPP}, by taking the integral given in (2.123) of the output noise PSD from $f_{START} = 1/T_{OPP}$ to 1GHz. The parameter γ for this design was γ=0.918mV/K. The integral was stopped at 1GHz because the total noise contribution at higher frequencies is negligible since the filter rolls of the high-frequency thermal noise contributions above 1GHz. Specifically, this integral was

$$T_{\left[1/T_{OPP},\,1GHz\right]} = \frac{1}{\gamma}\sqrt{\int_{1/T_{OPP}}^{1GHz}\left[\sum_{i=1}^{5}\left(\left|T_{i1}(j\omega)\right|^2 S_i\right)\right]df} \qquad (2.127)$$

The results are shown in Figure 2-23 where the time on the horizontal axis is the operation time, T_{OPP} .

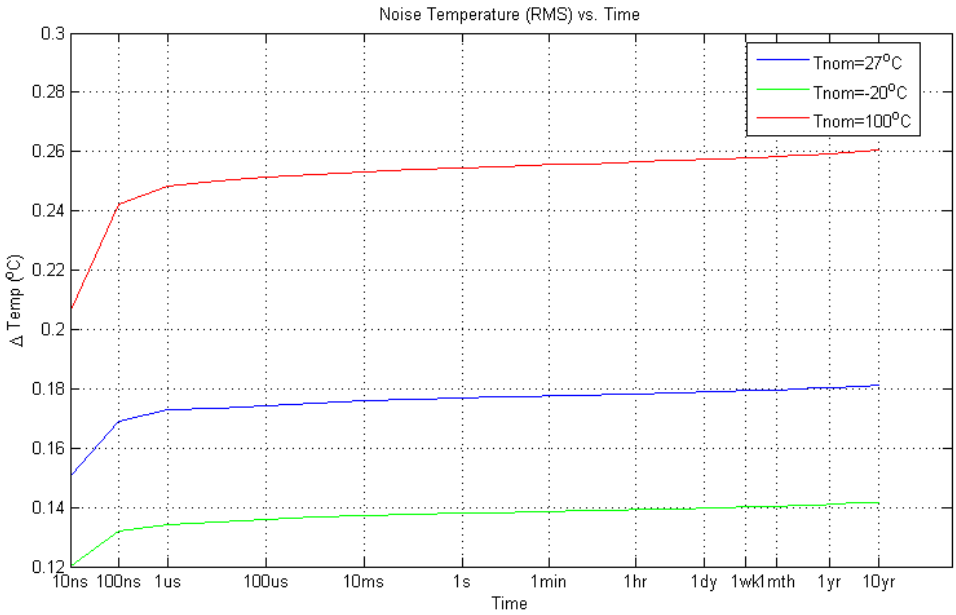


Figure 2-23: RMS noise temperature of the N-type 5T temperature sensor in time domain

From the plots, it can be inferred that the N-type 5T temperature sensor will have RMS noise temperature of 0.26°C over the period of 10 years if operated continuously at 100°C for the 10 years.. Its effects will be somewhat lower if operated at a lower average temperature. This shows that the flicker noise can affect the temperature sensing performance of the circuit below 1°C error. Hence, to keep the noise level down (e.g. as low as 10% of nominal 1°C error) and assuming that all noise sources are dominated by flicker noise, the transistors sizing must be large enough to appropriately limit the flicker noise spectral density. As such, trade-offs will be made to attain low noise while keeping the overall circuit area small.

CHAPTER 3 MULTI-THRESHOLD TRANSISTORS CELL FOR LOW VOLTAGE TEMPERATURE SENSING APPLICATIONS

A paper submitted to the 54th IEEE International Midwest Symposium on Circuits and Systems

Authors: Sheng-Huang Lee, Chen Zhao, Yen-Ting Wang, Randall Geiger, Degang Chen

3.1 ABSTRACT

A new Low Voltage CMOS temperature sensor with low supply sensitivity is introduced. Though operation over a large temperature range is possible, this structure is particularly useful in power/thermal management applications where a rather narrow temperature band is of most concern. The sensor is based upon a multi-threshold 4 transistor cell and uses the temperature dependence of the threshold voltages to sense temperature. The low headroom requirement of the structure allows for very low voltage operation or practical cascoding at nominal supply voltages to further reduce the supply voltage sensitivity. With proper device sizing, a very linear relationship between output voltage and temperature is achieved. Simulation results show that the temperature linearity is robustness to process variations and the cascoded implementation has excellent insensitivity to the power supply voltage. The circuit has been implemented in a 65nm digital process with multiple threshold voltages devices. Simulation results show a temperature nonlinearity of less than 0.5°C over the temperature range of 100~150°C.

3.2 INTRODUCTION

As feature sizes in new CMOS processes continue to decrease and circuit complexities increase, packaging densities and local power densities of many integrated circuits (ICs) are increasing. This increases the temperature either locally or across the die and causes changes in circuit performance. If the temperature becomes too high, the IC will fail and/or lifetime will be degraded. To manage these problems, on-chip power/thermal management that includes continuous on-chip monitoring of temperature at multiple critical locations on a die is becoming commonplace. Low cost, small die area, good accuracy, low power dissipation, and negligible self-heating are key requirements in these integrated temperature sensor arrays. Inherent in these requirements is minimal dependence on variations in the power supply voltage.

There are several methods to build an on-chip temperature sensor. The most tradition and most common approach exploits the temperature-dependent electrical characteristics of the pn-junction to generate a voltage or a current that varies with temperature [**22**]. Many of those reported consume substantial silicon area and have significant power requirements. Temperature sensors that utilize the temperature dependence of the threshold voltage of MOS transistors have also been discussed in the literature [**17**] [**23**]. Recently, a time-to-digital-converter based approach to measuring temperature was introduced. Those in this class discussed in [**24**] utilize the temperature dependence of both the CMOS threshold voltage and mobility to obtain the thermal information. The linearity of the time-to-digital converter based temperature sensor structures that have been reported is modest and the area required for the implementations is substantial.

In previous work [**17**] by the authors, a highly linear compact on-chip threshold voltage based temperature sensor using the reverse Widlar current mirror was introduced. An implementation of this structure in which a device sizing strategy that reduced 2nd and 3rd order temperature nonlinearity in the temperature transfer characteristics was discussed. Although the structure has low supply voltage sensitivity, it could be improved by increasing the output impedance of the current sources and cascoding the outputs is the most common way of doing this. Unfortunately, in low-voltage processes, there is not enough headroom in this structure for cascoding.

A low-voltage supply-insensitive 4-transistor CMOS threshold-based temperature sensor that relies on the temperature dependence of two NMOS (or PMOS) transistors with different threshold voltages that are native in newer digital processes is presented in this chapter. The temperature sensor is implemented in a 65nm digital process with native multiple threshold MOS devices. In contrast to most other threshold-based references and temperature sensors, the 4-transistor sensor has a single stable equilibrium point and thus does not require a start-up circuit. When operating at the nominal supply voltage of 1.2V in a 65nm process, the structure has enough excess voltage headroom for full cascoding. With cascoding, the 8-transistor (excluding biasing transistors) temperature sensor has even better supply insensitivity.

Architecturally, the 4-transistor dual-threshold cell has previously been used to realize a low voltage strong-inversion/weak-inversion temperature insensitive current reference [**25**] [**26**].

3.3 THRESHOLD VOLTAGE REFERENCE CIRCUIT

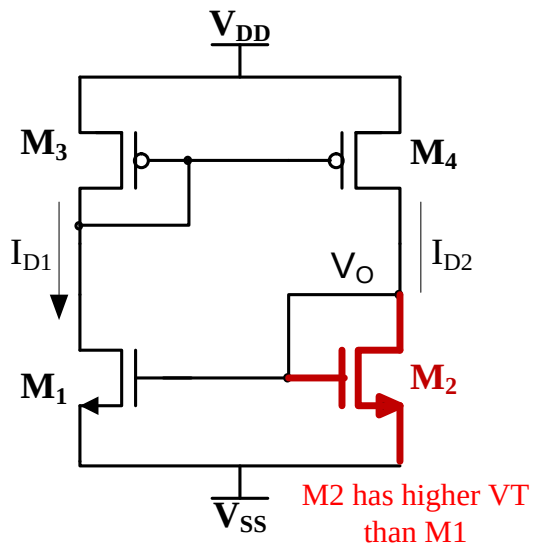


Figure 3-1: Schematic of proposed dual-VT temperature sensor circuit

The proposed temperature sensor is shown in Figure 3-1. This circuit is made functional by having two different threshold voltages in either the n-channel transistor pair or the p-channel transistor pair. In the following discussion, it will be assumed that the n-channel devices have different threshold voltages.

3.4 CIRCUIT ARCHITECTURE TRANSFER CHARACTERISTICS

The circuit in Figure 3-1 can be viewed as two cascaded inverters in a loop. In order to determine the stable operating point of the circuit, the loop can be broken at the VO node, as shown in Figure 3-2, and the analytical transfer characteristics of the cascaded inverter pair can be obtained. If the loop is broken between M_3 and M_4, similar transfer characteristics (referenced to V_{DD}) can be observed.

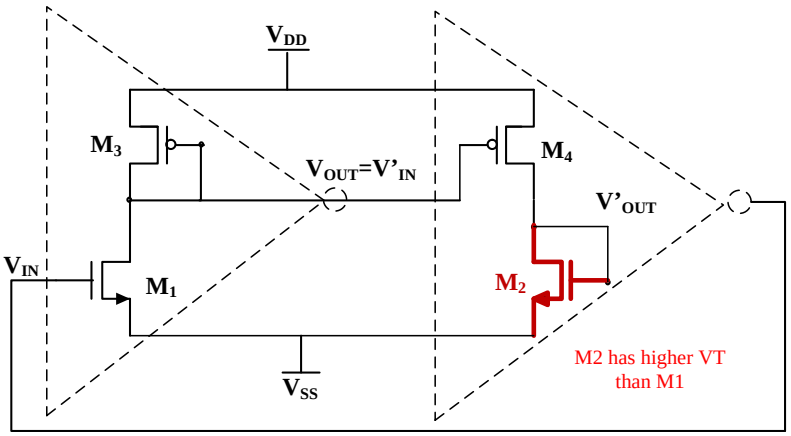


Figure 3-2: Cascade of n-channel/p-channel input inverters

Using the ideal square-law model and neglecting the output conductance effect, a straightforward analysis of the first inverter stage yields the following analytical expressions at 3 possible operation regions:

M_1 cutoff, M_3 saturated

$$V_{O1} = V_{DD} + V_{Tp}, \quad for \quad V_{IN} < V_{Tn} \tag{3.1}$$

M_1 saturated, M_3 saturated

$$V_{O1} = -\frac{V_{IN}}{\sqrt{\theta_1}} + V_{DD} + V_{Tp} + V_{Tn}\left(\frac{1}{\sqrt{\theta_1}}\right), \quad for \quad V_{Tn1} + (V_{DD} + V_{Tp3})\left(\frac{\sqrt{\theta_1}}{1+\sqrt{\theta_1}}\right) > V_{IN} > V_{Tn1} \tag{3.2}$$

M_1 triode, M_3 saturated; V_{OUT} satisfies the equation

$$V_{O1}^2\left(\frac{1+\theta_1}{2}\right) + V_{O1}\left(V_{Tn1} - V_{IN} - \theta_1\left[V_{DD} + V_{Tp3}\right]\right) + \left(\frac{\theta_1}{2}\left[V_{DD} + V_{Tp3}\right]^2\right) = 0 \quad \text{for} \quad V_{IN} > V_{Tn1} + (V_{DD} + V_{Tp3})\left(\frac{\sqrt{\theta_1}}{1+\sqrt{\theta_1}}\right) \tag{3.3}$$

where the parameter θ_1 is defined as

$$\theta_1 = \frac{W_3 L_1}{W_1 L_3} \frac{\mu_p}{\mu_n} \tag{3.4}$$

Similarly, the second inverter stage with an input $V_{IN2}=V_{O1}$ is governed by the following operation regions:

M_4 cutoff, M_2 saturated

$$V_O = V_{Tn2}, \quad for \quad V_{IN2} > V_{DD} + V_{Tp4} \tag{3.5}$$

M_4 saturated, M_2 saturated

$$\begin{aligned} V_O &= -\frac{V_{IN2}}{\sqrt{\theta_2}} + V_{Tn} + \left(V_{DD} + V_{Tp}\right)\left(\frac{1}{\sqrt{\theta_2}}\right), \\ V_{DD} + V_{Tp4} &> V_{IN2} > V_{Tp4} + V_{Tn2}\left(\frac{\sqrt{\theta_2}}{1+\sqrt{\theta_2}}\right) + V_{DD}\left(\frac{1}{1+\sqrt{\theta_2}}\right) \end{aligned} \tag{3.6}$$

M_4 triode, M_2 saturated; V_{OUT} satisfies the equation

$$\begin{aligned} &V_O^2\left(1+\theta_2\right) + V_O\left(-2\theta_2 V_{Tn2} - 2V_{IN2} + 2V_{Tp}\right) + \left(-2V_{DD}\left[\frac{V_{DD}}{2} - V_{IN2} + V_{Tp}\right] + \theta_2 V_{Tn}^2\right) = 0 \\ &for \quad V_{IN2} < V_{Tp4} + V_{Tn2}\left(\frac{\sqrt{\theta_2}}{1+\sqrt{\theta_2}}\right) + V_{DD}\left(\frac{1}{1+\sqrt{\theta_2}}\right) V_{DD} \end{aligned} \tag{3.7}$$

where the parameter θ_2 is defined as

$$\theta_2 = \frac{W_2 L_4}{W_4 L_2} \frac{\mu_n}{\mu_p} \tag{3.8}$$

The loop gain, A_{VL}, of the cascaded inverter pair is the product of the small signal voltage gain of each stage. When all transistors are operating in saturation, the individual gains are given by:

$$A_{V13} = \frac{g_{m1}}{g_{m3}} = \sqrt{\frac{W_1 L_3}{W_3 L_1} \cdot \frac{\mu_n}{\mu_p}} \tag{3.9}$$

$$A_{V42} = \frac{g_{m4}}{g_{m2}} = \sqrt{\frac{W_4 L_2}{W_2 L_4} \cdot \frac{\mu_p}{\mu_n}} \tag{3.10}$$

Then

$$A_{VL} = A_{V13} \cdot A_{V42} = \sqrt{\frac{W_1 L_3}{W_3 L_1} \cdot \frac{W_4 L_2}{W_2 L_4}} \tag{3.11}$$

The operating point of the two inverter loop is at the intersection of the transfer characteristics of the two inverters and the unity slope line defined by $V_{O2}=V_{IN}$. If more than one intersection occurs, a start-up circuit is needed to select a single stable equilibrium point. To maintain a low sensitivity to the supply voltage in this circuit, it is necessary that all transistors are operating in the saturation region. The transfer characteristics of the inverter pair will now be considered under two scenarios; when the n-channel transistors are the same and when they are different.

3.4.1 Single Threshold Voltage

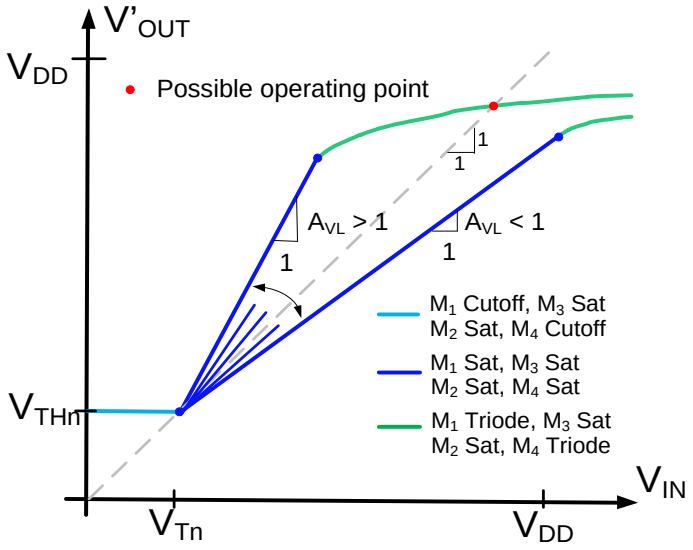


Figure 3-3: Transfer characteristics of inverter pair with single n-channel threshold voltage

In the first scenario, assume that the threshold voltage of the n-channel input transistor of the first inverter, V_{THn1} to be equal to the n-channel load transistor of the second inverter, V_{THn2}. The threshold voltages for both p-channel transistors are also assumed to be equal to each other. Figure 3-3 shows the resulting transfer characteristics under different sizing conditions. For a saturation region loop gain of less than 1, the transfer curve only intersects with the unity loop gain locus at V_{IN} equals to V_{THn1}, which is not a viable operating point because the transistors are operating in the weak-inversion or cutoff region. For loop gain of more than 1, the transfer curve intersects at two points; one when the transistors are cutoff and the other when one of the transistors is in the triode region. The latter intersection is not a viable operating point because one of the transistors is operating in the triode region which will not provide the required low sensitivity to V_{DD}.

3.4.2 Dual Threshold Voltage

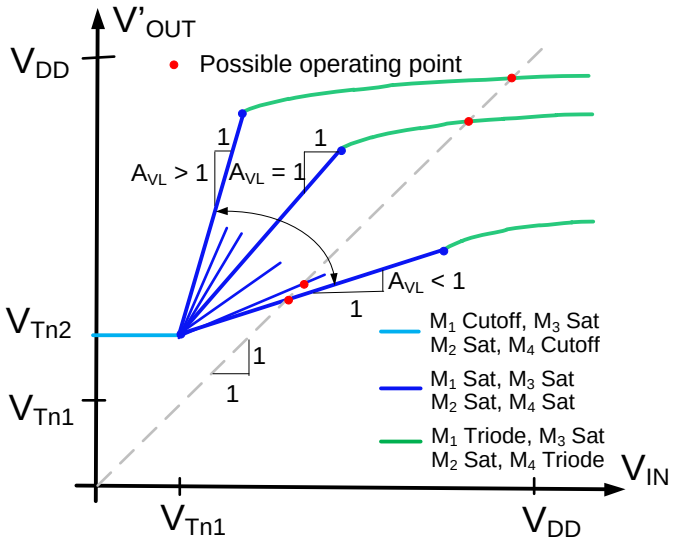


Figure 3-4: Transfer characteristics of inverter pair with dual n-channel threshold voltage ($V_{Tn1}<V_{Tn2}$)

In the second scenario, the threshold voltage of the n-channel input transistor of the first inverter, V_{THn1}, is selected to be less than that of transistor M_2. The threshold voltages for the p-channel transistors are again assumed to be equal to each other. Figure 3-4 shows the resulting transfer characteristics of the inverting pair with two different n-channel threshold voltages. For a saturation region loop gain that is larger than 1, the transfer curve has a unique intersection point on the unity loop gain curve but at this intersection one or more transistors are operating in triode region. As in the previous scenario, this is not a practical design because the sensitivity to V_{DD} will be large. For a saturation region loop gain that is less than 1, there exists a unique intersection point between with the unity loop gain locus where all transistors are operating in the saturation region. This provides a useful operating point in which the output node voltage is insensitive to V_{DD}. In addition, since there is only one stable equilibrium point in this case, there is no need for a startup circuit to establish the desired operating point.

The threshold voltage difference will be dictated dominantly by what devices are available in a process though bulk bias may also be used advantageously to help manage the threshold differences. In general, small threshold differences will require saturation region gains close to unity resulting in high sensitivities to model and design parameters whereas design constraints will be relaxed if the threshold differences.

3.5 THRESHOLD VOLTAGE REFERENCED OUTPUT

The output voltage for the 4-transistor temperature sensor of Figure 3-1 will now be derived. Assuming a square-law model and ignoring output conductance effects, the left and right branches have drain currents given by the expressions:

$$I_{D1} = \frac{\mu_n C_{ox}}{2} \frac{W_1}{L_1} (V_O - V_{Tn1})^2 \tag{3.12}$$

$$I_{D2} = \frac{\mu_n C_{ox}}{2} \frac{W_2}{L_2} (V_O - V_{Tn2})^2 \tag{3.13}$$

$$I_{D1} = M I_{D2} \tag{3.14}$$

where M is the current-mirror gain of the p-channel transistors pair.

A set of three simultaneous equations (3.12)–(3.14) with the unknown variables {I_{D1}, I_{D2}, and V_O} are then solved to obtain an expression of V_O:

$$V_O = \frac{\sqrt{W_1/L_1}}{\left(\sqrt{W_1/L_1} - \sqrt{M\,W_2/L_2}\right)} V_{Tn1} - \frac{\sqrt{M\,W_2/L_2}}{\left(\sqrt{W_1/L_1} - \sqrt{M\,W_2/L_2}\right)} V_{Tn2} \tag{3.15}$$

From (3.15), it can be observed that the output voltage is a weighted linear difference between the threshold voltages V_{THn1} and V_{THn2} and is independent of V_{DD}.

The temperature dependent threshold voltage model that is widely used in circuit simulators [**19**] is given in (3.16)

$$V_{TH}(T) = V_{TH}(TNOM) + \left(KT1 + \frac{KT1L}{L_{eff}} + KT2 \cdot V_{bseff} \right) \cdot \left(\frac{T}{TNOM} - 1 \right) \qquad (3.16)$$

where TNOM is the nominal temperature usually set at 300K; KT1, KT1L, and KT2 are process dependent constants; L_{eff} is the effective length, and V_{bseff} is the effective bulk to source voltage. Circuit implementations may result in a weak temperature dependence of V_{bseff} but in the temperature sensor of Figure 3-1, all bulks are source connected. Thus, in this circuit, if follows from (3.15) and (3.16) that with the simplified square law model, the output voltage is linearly dependent on temperature and thus this circuit serves as a linear temperature sensor. The finite output impedance of the device degrades linearity and introduces a modest V_{DD} sensitivity. Analytical expressions for the effects of output impedance on linearity are unwieldy.

3.6 DESIGN FOR HIGH TEMPERATURE SENSING APPLICATIONS

Two temperature sensor circuits (regular and cascode) based upon the 4-transistor cell of Figure 3-1 were designed in a 65nm multiple-VT digital process. The nominal supply voltage in the process is 1.2V. The sensor was designed to operate in the high temperature range between 100°C and 150°C. The nominal temperature was defined to be 125°C. The

nonlinear error of the sensor, expressed in °C, is the difference in the measured temperature and the end-point fit line temperature. The temperature integral nonlinearity error (TINL) in °C at the output node of the sensor is defined as

$$TINL = \left[\max_{100^oC<T<150^oC} \left| V_o(T) - V_{OFIT}(T) \right| \right] \left(\frac{50^oC}{V_0(150^oC) - V_0(100^oC)} \right) \tag{3.17}$$

where $V_{OFIT}(T)$ is the output end-point fit line to the two points $V_O(100°C)$ and V_O (150°C).

3.6.1 Devices Sizing Strategy

Given the availability of multiple-VT devices in the CMOS process, a low-VT NMOS for M_1 and a high-VT NMOS for M_2 are chosen, such that the threshold voltages V_{Tn1} and V_{Tn2} are as far apart as possible. The PMOS pair for the current mirror, M_3 and M_4 will use devices of the same VT. To achieve loop gain of less than 1, we set the current mirror PMOS pair W/L ratio to be at least 3 times larger than the largest of M_1 and M_2 based on (9) and (10), assuming that the mobility ratio of the electrons to the holes is approximately 3. Both M_1 and M_2 NMOS device sizing will determine the current level of the circuit such that the total current will decrease for smaller W_1/L_1 and larger W_2/L_2, and vice versa. A good suggested starting point is to set both output node voltages to be near $V_{DD}/2$, such that both the V_{DS} of NMOS and PMOS are large to keep them in strong inversion. This can be done by adjusting the loop gain of each branch.

To reduce the temperature nonlinearity of the circuit, a numerical optimization procedure can be operated as follows:

I. Vary W_2 by a certain amount ΔW_2, such as 20% of the initial size, and find out the sensitivity of output temperature error with respect to the width's change. If the error decreases, replace the initial W_2 with the new value.

II. Similarly, vary W1 using the approach in step I.

III. Repeat step I and II alternately that will lead to a local minimum of the temperature error. Keep watch of the nominal current level of the circuit as the sizing variation of M_1 and M_2 may drastically increase or decrease the total current level.

IV. Iterate step III as many times necessary until the temperature error does not have significant improvement. Then, consider tuning the size of the PMOS current-mirror and scaling the lengths of M_1 and M_2.

3.6.2 4-transistors N-Type Temperature Sensor

Device sizes for a realization of the 4-transistor temperature sensor are given in Table 3-1. Process corner simulations and supply variations were run to predict linearity robustness over process and supply variations compared to typical (TT) operation. Results appear in Figure 3-5. Corners are designated as (FF: Fast NMOS Fast PMOS, SS: Slow NMOS Slow PMOS, FS: Fast NMOS Slow PMOS, SF: Slow NMOS Fast PMOS) and ±10% supply variations around nominal V_{DD} of 1.2V as (L=Low, N=Nominal, H=High).

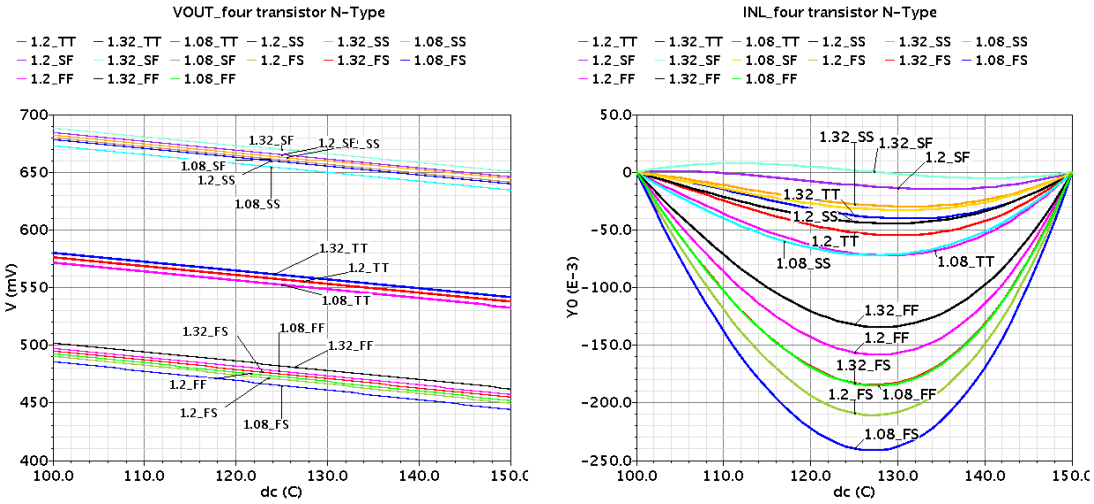


Figure 3-5: Simulated 4T (a) output voltage and (b) temperature error at different process corners and ±10% variation over nominal V_{DD} of 1.2V

The maximum temperature nonlinearity error at typical conditions is 0.0546°C across the temperature range between 100°C and 150°C and the worst-case maximum temperature error of 0.24°C occurs at the FS corner with a low supply voltage. The nominal temperature coefficient is -0.77mV/°C.

At TT, the maximum output variation with ±10% supply voltage variation is 9.18mV. This level of supply variation would cause an additional and much larger temperature error of 11.9°C if VDD varies with time, i.e. noisy supply due to digital switching, temperature dependent supply etc. This is due primarily to the limited output impedance of the MOS transistor.

The transfer characteristics of the 4-transistors circuit are also simulated over all process corners and V_{DD} variation of ±10%, as shown in Figure 3-6. Looking at the family of curves, it seems that there is always a single crossing point with the unity loop gain locus. This shows that the circuit has only one stable equilibrium point over all process corners and V_{DD} variation, thus startup circuit is not required.

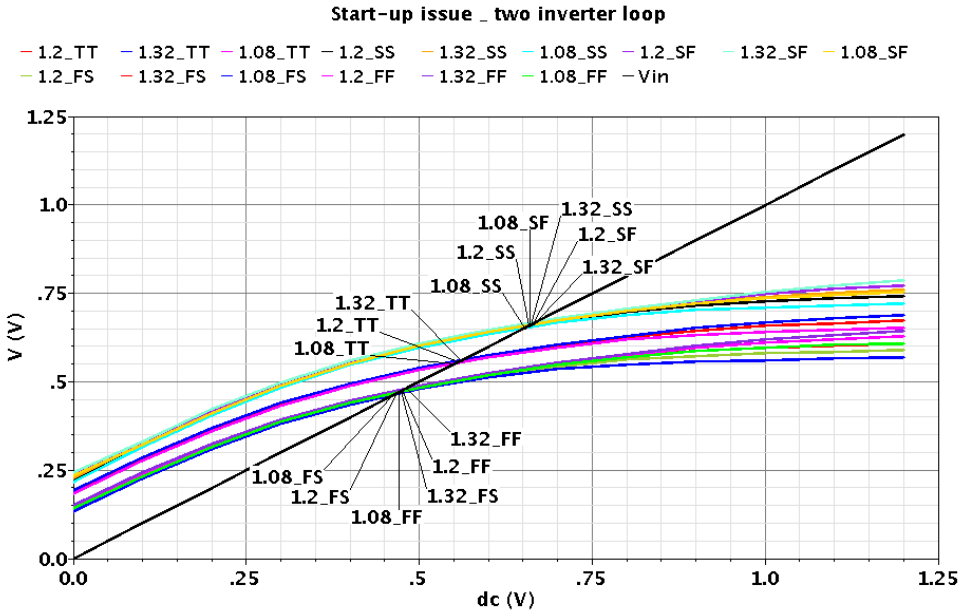


Figure 3-6: Simulated transfer characteristics of the 4T temperature sensor

3.6.3 Cascode N-Type Temperature Sensor

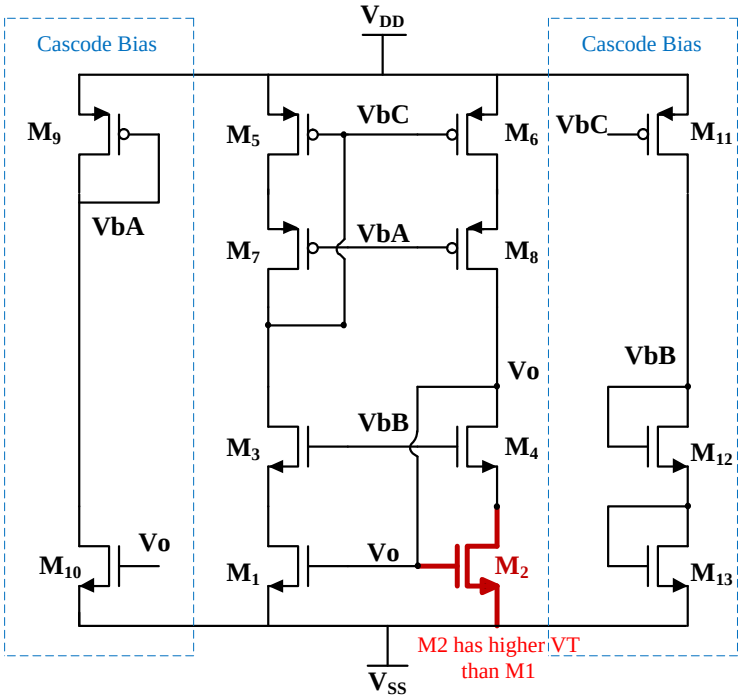


Figure 3-7: Schematic of cascode temperature sensor with biasing transistors

The circuit of Figure 3-1 has enough headroom to allow for complete cascoding. This will significantly reduce the supply voltage sensitivity. A complete schematic of the cascoded n-type temperature sensor including bias generators is shown in Figure 3-7.

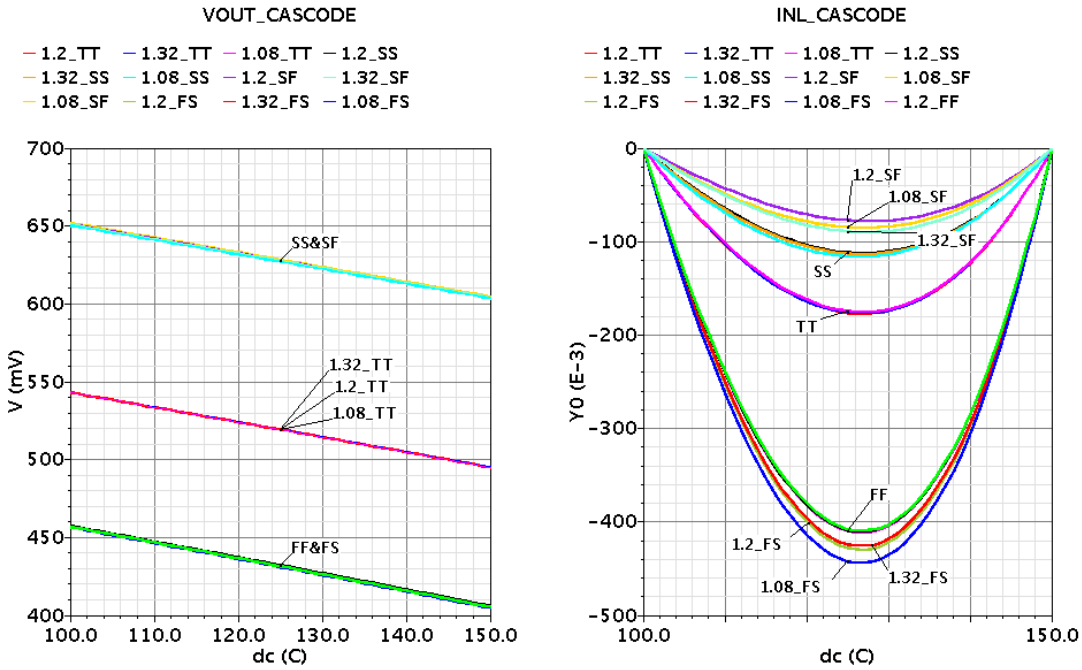


Figure 3-8: Simulated cascode (a) output voltage and (b) temperature error at different process corners and ±10% variation over nominal VDD of 1.2V

Device sizes for an implementation of the cascode temperature sensor are given in Table 3-1. The cascode circuit was simulated under the same conditions as the 4-transistors circuit and the results are shown in Figure 3-8. The maximum temperature error at TT is 0.18°C over the temperature range between 100°C and 150°C. The worst-case maximum temperature error of 0.44°C over process and supply variations occurs at the FS corner with a low supply voltage. At TT, the maximum output voltage variation is 314µV and this would introduce an additional temperature error of 0.33°C if V_{DD} varies ±10% from its nominal value.

In addition, the noise performance of the 4-transistors cell is investigated. Detailed derivations can be found in Appendix 3B. The noise spectral density is shown in Figure 3-9.

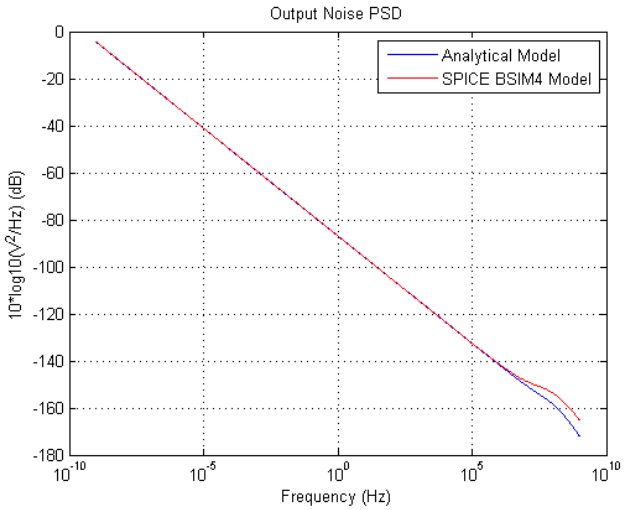


Figure 3-9: Output noise power spectral density for multi-VT 4T temperature sensor

The time-domain noise performance plot is then obtained by taking the integral of the output noise PSD from 10MHz to range of frequencies corresponding to the equivalent time periods. The results are shown in Figure 3-10.

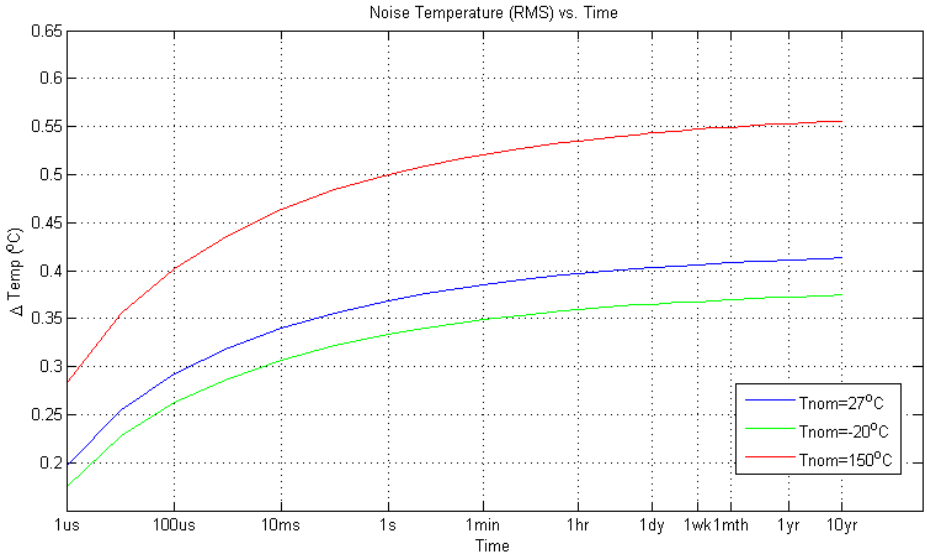


Figure 3-10: RMS noise temperature of the multi-VT 4T temperature sensor in time domain

From the plots, it can be inferred that the multi-VT 4T temperature sensor will have RMS noise temperature of 0.56°C over the period of 10 years. This shows that the flicker noise is quite high for small feature size process and can significantly affect the temperature sensing performance (56% of 1°C error). Hence, the transistors size cannot be too small, thus compromise must be made for small-area design.

Overall performance of the two temperature sensors is shown in Table 3-1. It can be seen that the active area is very small and the total power dissipation is very low.

These simulation results are based upon the linear temperature dependent model of the threshold voltage that is widely used in many simulators. Some higher-order nonlinearities in the temperature dependence of the threshold voltage do exist and will cause additional degradation in linearity.

3.7 CONCLUSIONS

A low-voltage supply-insensitive 4-transistor CMOS threshold-based temperature sensor that relies on the temperature dependence of two NMOS (or PMOS) transistors with different threshold voltages was introduced. A fully cascoded extension of this circuit was presented that has even lower power supply sensitivity. Neither structure requires a start-up circuit. The active area of both structures is small and the power dissipation is also very low. Simulation results suggest that these structures can be used as temperature sensors for power/thermal management.

Table 3-1: Summary of Performance

Specification	**Performance**	
Process	65nm	
Voltage Supply	1.2V	
Temperature Range	100~150˚C	
Parameter	**4T**	**Cascode**
Estimated Active Area (μm^2)	54	96
Nominal power consumption (μW)	11.0	5.12
Temperature Coefficient (mV/ ˚C)	-0.77	-0.96
Max. Temp. INL (˚C) at Typical	0.055	0.18
Max. Temp. INL (˚C) at Worst Case	0.24	0.44
Supply Sensitivity over ±10% Variation at Typical (˚C)	11.9	0.33
Sizing Information		
4T sizing (μm): W_1(0.3), W_2(4.8), $W_{3,4}$(1.5), All L(1)		
Cascode sizing (μm): W/L_1(0.15/2.5), W/L_2(3.2/4), $W/L_{3,4}$(0.15/0.3), $W/L_{5,6}$(0.15/0.25), $W/L_{7,8}$(0.75/0.25)		

APPENDIX 3A POWER SUPPLY EFFECTS ON INTEGRATED MULTI-VT TEMPERATURE SENSORS

In this appendix an analytical formulation of the effects of the supply voltage on the temperature output of the multi-VT 4-transistors circuit will be discussed.

BASIS MULTI-VT TEMPERATURE SENSOR ANALYSIS

Consider initially the temperature sensor shown in Figure 3-11. A small-signal equivalent circuit that will be used to determine the effects of supply voltage variations on the temperature sensor output is shown in Figure 3-12.

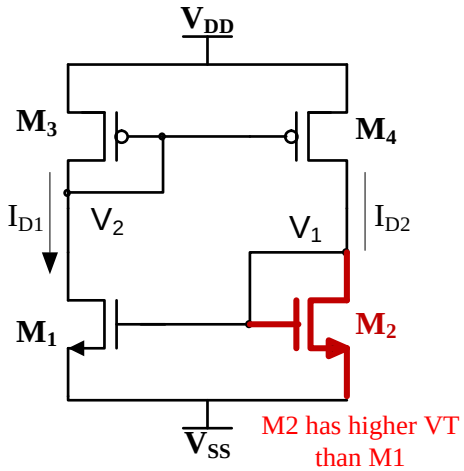


Figure 3-11: Basis multi-VT temperature sensor

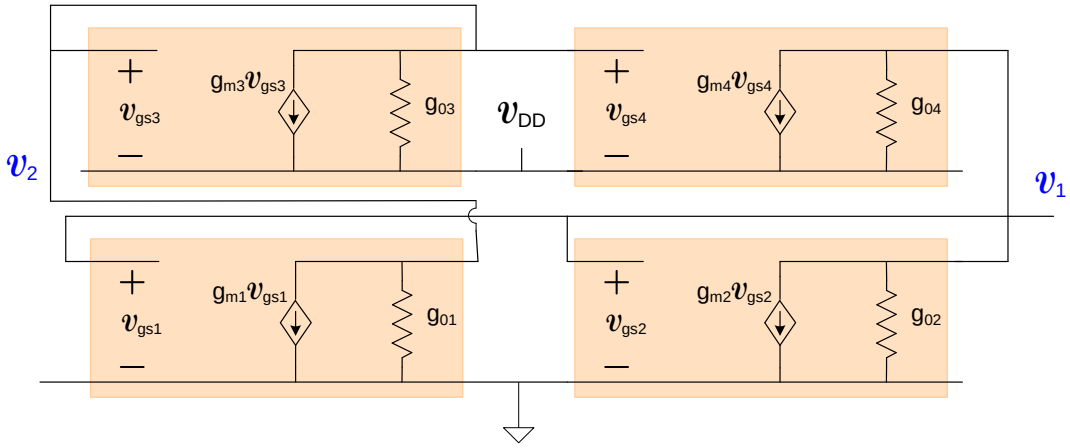


Figure 3-12: Small-signal equivalent temperature sensor of Figure 3-11

In the following analysis, a script font will be used to denote small-signal voltage variables.

It follows from KCL that:

$$\left.\begin{aligned} \mathcal{v}_1\left(g_{o2}+g_{o4}\right)+g_{m2}\mathcal{v}_{gs2}+g_{m4}\mathcal{v}_{gs4}&=g_{o4}\mathcal{v}_{DD}\\ \mathcal{v}_2\left(g_{o1}+g_{o3}\right)+g_{m1}\mathcal{v}_{gs1}+g_{m3}\mathcal{v}_{gs3}&=g_{o3}\mathcal{v}_{DD}\end{aligned}\right\} \tag{3.18}$$

In these equations, the gate-source voltages are given by

$$\left.\begin{aligned} \mathcal{v}_{gs1}&=\mathcal{v}_1\\ \mathcal{v}_{gs2}&=\mathcal{v}_1\\ \mathcal{v}_{gs3}&=\mathcal{v}_2-\mathcal{v}_{DD}\\ \mathcal{v}_{gs4}&=\mathcal{v}_2-\mathcal{v}_{DD}\end{aligned}\right\} \tag{3.19}$$

Substituting (3.19) into (3.18), two equations are obtained.

$$\left.\begin{aligned} \mathcal{v}_1\left(g_{o2}+g_{o4}\right)+g_{m2}\mathcal{v}_1+g_{m4}\left(\mathcal{v}_2-\mathcal{v}_{DD}\right)&=g_{o4}\mathcal{v}_{DD}\\ \mathcal{v}_2\left(g_{o1}+g_{o3}\right)+g_{m1}\mathcal{v}_1+g_{m3}\left(\mathcal{v}_2-\mathcal{v}_{DD}\right)&=g_{o3}\mathcal{v}_{DD}\end{aligned}\right\} \tag{3.20}$$

These can be rewritten as

$$\left.\begin{aligned} v_1\left(g_{m2}+g_{o2}+g_{o4}\right)+g_{m4}v_2 &= \left(g_{m4}+g_{o4}\right)v_{DD} \\ v_2\left(g_{m3}+g_{o1}+g_{o3}\right)+g_{m1}v_1 &= \left(g_{m3}+g_{o3}\right)v_{DD} \end{aligned}\right\} \tag{3.21}$$

Eliminating v_2 yields the single equation

$$v_1\left(\frac{g_{m2}+g_{o2}+g_{o4}}{g_{m4}}-\frac{g_{m1}}{g_{m3}+g_{o1}+g_{o3}}\right)=\left(\frac{g_{m4}+g_{o4}}{g_{m4}}-\frac{g_{m3}+g_{o3}}{g_{m3}+g_{o1}+g_{o3}}\right)v_{DD} \tag{3.22}$$

This can be solved to obtain the expression

$$\frac{v_1}{v_{DD}}=\frac{\left(g_{m4}+g_{o4}\right)\left(g_{m3}+g_{o1}+g_{o3}\right)-g_{m4}\left(g_{m3}+g_{o3}\right)}{\left(g_{m2}+g_{o2}+g_{o4}\right)\left(g_{m3}+g_{o1}+g_{o3}\right)-g_{m1}g_{m4}} \tag{3.23}$$

Expanding the expression then yields

$$\frac{v_1}{v_{DD}}=\frac{g_{m3}g_{o4}+g_{m4}g_{o1}+g_{o4}\left(g_{o1}+g_{o3}\right)}{g_{m2}\left(g_{m3}+g_{o1}+g_{o3}\right)+g_{m3}\left(g_{o2}+g_{o4}\right)-g_{m1}g_{m4}+\left(g_{o2}+g_{o4}\right)\left(g_{o1}+g_{o3}\right)} \tag{3.24}$$

It is difficult to get much insight into how large this gain or attenuation is because of the high level of interdependence between the small signal variables in (3.24). It will now be assumed that all output conductances are small compared to any transconductances in the numerator and denominator given in (3.24). Of course, there is some risk at making this assumption since a difference of two functions appears in the denominator of (3.24). So, after making this assumption, it will be necessary to show that the difference in the denominator of (3.24) is large compared to the output conductances.

With this assumption, it follows that

$$\frac{v_1}{v_{DD}} \simeq \frac{g_{m3}g_{o4} + g_{m4}g_{o1}}{g_{m2}g_{m3} - g_{m1}g_{m4}} \tag{3.25}$$

A relation between the large signal and small signal parameters will now be made.

Specifically, for each device it will be assumed that

$$g_o = \lambda I_{DQ} \tag{3.26}$$

$$g_m = \frac{2I_{DQ}}{V_{EB}} \tag{3.27}$$

where I_{DQ} is the quiescent drain current and V_{EB} is the quiescent excess bias voltage. Now define the mirror gain of the p-channel current mirror to be M. It thus follows that

$$I_{D2Q} = MI_{D1Q} \tag{3.28}$$

The excess bias voltages of the n-channel transistors can be expressed as

$$V_{EB1} = V_{1Q} - V_{THn1} \tag{3.29}$$

$$V_{EB2} = V_{2Q} - V_{THn2} \tag{3.30}$$

where V_{1Q} and V_{2Q} are the quiescent values of the voltages V_1 and V_2.

Substituting from (3.26), (3.27), (3.28), (3.29) and (3.30) into (3.25) yields

$$\frac{v_1}{v_{DD}} \simeq \frac{\frac{1}{V_{EB3}}\lambda_4 + \frac{1}{V_{EB4}}\lambda_1}{2\left(\frac{1}{V_{EB2}V_{EB3}} - \frac{1}{V_{EB1}V_{EB4}}\right)} \tag{3.31}$$

Assuming that M_3 and M_4 are matched to achieve mirror gain M=1, the following expression is obtained:

$$\frac{v_1}{v_{DD}} \simeq \frac{\lambda_4 + \lambda_1}{2\left(\frac{1}{V_{EB2}} - \frac{1}{V_{EB1}}\right)} \tag{3.32}$$

For convenience define the parameter α as

$$\alpha = \frac{V_{EB2}}{V_{EB1}} = \frac{V_{1Q} - V_{THn2}}{V_{1Q} - V_{THn1}} \tag{3.33}$$

It thus follows that

$$\frac{v_1}{v_{DD}} \simeq \frac{(\lambda_4 + \lambda_1)V_{EB1}}{2\left(\frac{1-\alpha}{\alpha}\right)} \tag{3.34}$$

The parameter α is generally much less than 1 (for $V_{THn2} > V_{THn1}$) so the denominator in (3.34) is not small, justifying the assumption that we could neglect all g_o terms in the denominator of (3.24).

It might be useful to provide a bit more insight into what (3.34) shows. This equation can be expressed equivalently as

$$\frac{v_1}{v_{DD}} \simeq \frac{(\lambda_4 + \lambda_1)V_{EB1}}{2\left(\frac{1-\alpha}{\alpha}\right)} = \left(\frac{\alpha}{1-\alpha}\right)\frac{(\lambda_4 + \lambda_1)I_{D1Q}V_{EB1}}{2I_{D1Q}} \tag{3.35}$$

If we assume that $\lambda_1=\lambda_4=\lambda$, it follows that

$$\frac{v_1}{v_{DD}} \simeq \left[\frac{\alpha}{1-\alpha}\right]\frac{2\left(\lambda I_{D1Q}\right)}{\left(\frac{2I_{D1Q}}{V_{EB1}}\right)} = 2\left[\frac{\alpha}{1-\alpha}\right]\frac{g_{o1}}{g_{m1}} \tag{3.36}$$

We thus have a relationship between the power supply gain and the small signal parameters which is repeated as:

$$\frac{v_1}{v_{DD}} \simeq 2\left[\frac{\alpha}{1-\alpha}\right]\frac{g_{o1}}{g_{m1}} \tag{3.37}$$

This power supply gain can be quite small provided α is not too close to 1. But it can be made really small by a judicious design choice of α. The magnitude of the coefficient of g_{o1}/g_{m1} in (3.37) for different values of α is shown in Figure 3-13.

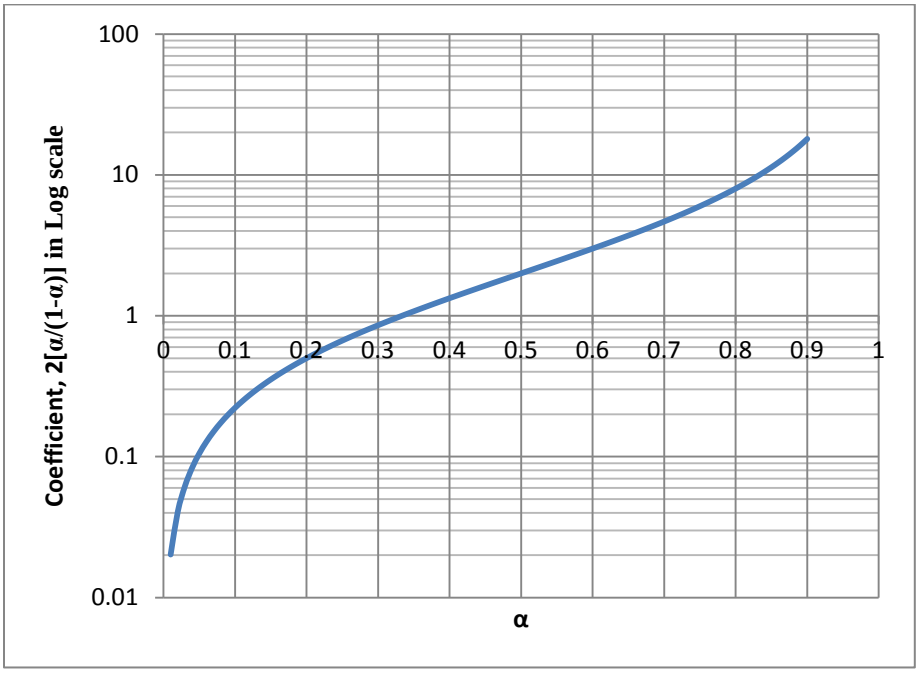


Figure 3-13: Magnitude of coefficient in (3.37)

From the plot, it can be observed that when α is less than 0.33, the magnitude of the coefficient will be less than 1. Since the term g_{o1}/g_{m1} in (3.37) is typically much less than 1, it follows from (3.33) that we will have better V_{DD} insensitivity if we set $V_{EB2} < 0.3V_{EB1}$.

Although the magnitude of the power supply gain can be made quite small by judicious choice of the parameter α, it can be made much smaller by cascoding. And, if cascoding is used, the constrains on α can be relaxed. Cascoding is discussed in the following section.

CASCODED MULTI-VT TEMPERATURE SENSOR ANALYSIS

The issue of cascoding also deserves attention. Although cascoding decreases the supply voltage headroom budget, it can be shown that the 4-transistor temperature sensor of Figure 3-11 has enough headroom that full cascoding is practical even when operating with very low supply voltages. A fully-cascoded variant of the multi-VT 4-transistor temperature sensor is shown in Figure 3-14 where all transistors have been cascoded. Note that full cascoding is not necessary as from (3.25), cascoding only transistors M_1 and M_4 is sufficient to derive near maximum benefit and still have a bit more headroom.

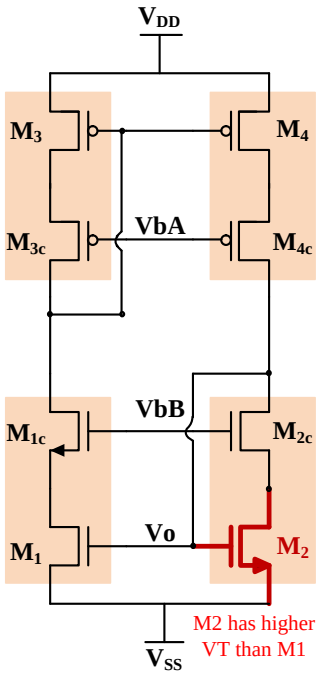


Figure 3-14: Cascoded Multi-VT Temperature Sensor

The cascoded transistor pairs have an equivalent small-signal transconductance and output conductance given by

$$g_{mcc} = g_m \tag{3.38}$$

$$g_{occ} = g_o\left(\frac{g_{oc}}{g_{mc}}\right) \tag{3.39}$$

It thus follows directly from (3.25) that the output voltage for the cascoded structure can be expressed as

$$\frac{v_1}{v_{DD}} \simeq \frac{g_{m3}g_{o4}\left(\frac{g_{o4c}}{g_{m4c}}\right) + g_{m4}g_{o1}\left(\frac{g_{o1c}}{g_{m1c}}\right)}{g_{m2}g_{m3} - g_{m1}g_{m4}} \tag{3.40}$$

In terms of the large signal operating parameters, it follows that

$$\frac{v_1}{v_{DD}} \simeq \frac{\frac{\lambda_4\lambda_{4c}V_{EB4c}}{V_{EB3}} + \frac{\lambda_1\lambda_{1c}V_{EB1c}}{V_{EB4}}}{4\left(\frac{1}{V_{EB2}V_{EB3}} - \frac{1}{V_{EB1}V_{EB4}}\right)} \tag{3.41}$$

Assuming that M_3 and M_4 are matched to achieve mirror gain M=1, the following expression is obtained:

$$\frac{v_1}{v_{DD}} \simeq \frac{\lambda_4\lambda_{4c}V_{EB4c} + \lambda_1\lambda_{1c}V_{EB1c}}{4\left(\frac{1}{V_{EB2}} - \frac{1}{V_{EB1}}\right)} \tag{3.42}$$

As expected, the cascoding reduces the gain from V_{DD} significantly.

If assuming that $\lambda_1=\lambda_4=\lambda_{1c}=\lambda_{4c}=\lambda$ and $V_{EB1}=V_{EB1c}=V_{EB4}=V_{EB4c}$, and defining the parameter α as in (3.33), it follows that:

$$\frac{v_1}{v_{DD}} \simeq \frac{\lambda^2\left(V_{EB4}+V_{EB1}\right)V_{EB1}}{4\left(\frac{1}{\alpha}-1\right)} = 2\frac{\left(\lambda^2 I_{D1Q}^2\right)}{\left(\frac{1}{\alpha}-1\right)}\left(\frac{V_{EB1}^2}{4I_{D1Q}^2}\right) \tag{3.43}$$

This can now be expressed in terms of small signal parameters as

$$\frac{V_1}{V_{DD}} \simeq 2\left[\frac{\alpha}{1-\alpha}\right]\left(\frac{g_{o1}}{g_{m1}}\right)^2 \tag{3.44}$$

The gain from V_{DD} is decreased by approximately a factor of g_{o1}/g_{m1} compared to what was obtained in the original 4-transistor circuit.

As discussed in Appendix 2A, the dc biasing voltages for the cascode transistors need to be generated and the biasing circuits themselves may be affected by the supply voltage variation. Fortunately, it can be shown that there are practical cascode biasing circuits in which the gain from the biasing voltage on the gates of the cascode transistors to the output is quite small One method of generating the cascode biasing voltages is to use the self-bias approach whereby currents from the core sensor itself are mirrored to a biasing circuit to form the biasing voltages. This is one practical method for biasing characterized by low sensitivity from the supply voltage to the cascode biasing voltages. This approach to biasing is discussed in the appendix to Chapter 4. Of course, with this approach, it is necessary to verify that the self-biasing circuit does not introduce multiple stable equilibrium points.

APPENDIX 3B NOISE ANALYSIS ON MULTI-VT TEMPERATURE SENSOR

The analysis in this appendix is similarly to that which was presented in Appendix 2B. Essentially the approach for the 5-transistor temperature is adapted to be applicable to the multi-VT 4-transistor sensor in this appendix. Since only four transistors comprise this temperature sensor, the noise analysis is actually somewhat less involved.

FREQUENCY-DEPENDENT NOISE CHARACTERIZATION OF MULTI-VT TEMPERATURE SENSOR

A small-signal equivalent circuit that includes the parasitic capacitances and the device noise sources is shown in Figure 3-15.

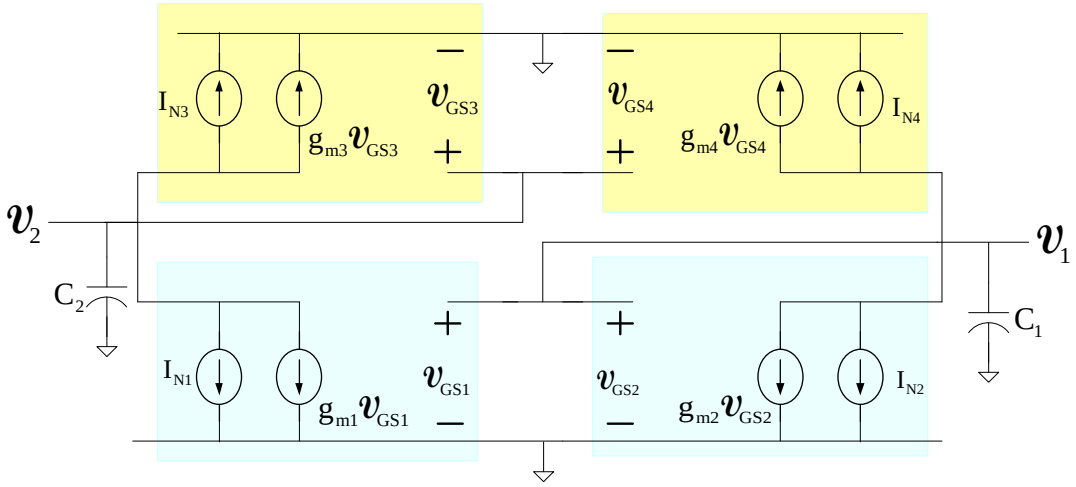


Figure 3-15: Frequency dependent noise model of the multi-VT 4T temperature sensor

Applying KCL at the two nodes, the following equations are obtained.

$$\left.\begin{aligned}(g_{m2}+sC_1)v_1+g_{m4}v_2+I_{N2}+I_{N4}=0\\ g_{m1}v_1+(g_{m3}+sC_2)v_2+I_{N1}+I_{N3}=0\end{aligned}\right\} \tag{3.45}$$

Eliminating v_2 yields

$$\left(\frac{g_{m2}+sC_1}{g_{m4}}-\frac{g_{m1}}{g_{m3}+sC_2}\right)v_1-\frac{1}{g_{m3}+sC_2}I_{N1}+\frac{1}{g_{m4}}I_{N2}-\frac{1}{g_{m3}+sC_2}I_{N3}+\frac{1}{g_{m4}}I_{N4}=0 \quad (3.46)$$

Hence, v_1 as a function of the noise sources can be expressed as

$$v_1=\frac{g_{m4}\left[I_{N1}+I_{N3}\right]-\left(g_{m3}+sC_2\right)\left[I_{N2}+I_{N4}\right]}{\left(g_{m2}+sC_1\right)\left(g_{m3}+sC_2\right)-g_{m1}g_{m4}} \quad (3.47)$$

Rearranging the terms to be expressed as ratios yields

$$v_1=\left[\frac{I_{N1}+I_{N3}-\left(\frac{g_{m3}+sC_2}{g_{m4}}\right)\left[I_{N2}+I_{N4}\right]}{\left(\frac{g_{m2}+sC_1}{g_{m1}}\right)\left(\frac{g_{m3}+sC_2}{g_{m4}}\right)-1}\right]\left(\frac{1}{g_{m1}}\right) \quad (3.48)$$

Although this expression is quite manageable, it is difficult to generate much insight into how the design variables in a circuit affect the output noise voltage since this expression involves correlated small-signal parameters. In what follows, I will now focus on writing (3.48) in a way that provides more insight into the actual noise performance.

Based on the design process of the temperature sensor, the current on each branch is set such that

$$I_{D2Q}=I_{D4Q}=MI_{D1Q}=MI_{D3Q} \quad (3.49)$$

where M is the gain of the p-channel current mirror. The currents can also be expressed in terms of Power and V_{DD}:

$$I_{D1Q} = \frac{P}{V_{DD}}\left(\frac{1}{1+M}\right) \tag{3.50}$$

The small-signal transconductance ratios can be expressed as:

$$\frac{g_{m2}}{g_{m1}} = \frac{MV_{EB1}}{V_{EB2}} = \sqrt{\frac{MW_2L_1}{W_1L_2}} \tag{3.51}$$

$$\frac{g_{m3}}{g_{m4}} = \frac{1}{M} \quad \text{since } V_{EB3} = V_{EB4} \tag{3.52}$$

Assuming that the gate-source capacitance of the devices, C_{GS} , are the dominate contributors to C_1 and C_2, we obtain the expressions

$$C_1 = C_{GS1} + C_{GS2} \tag{3.53}$$

$$C_2 = C_{GS3} + C_{GS4} \tag{3.54}$$

Several small-signal expressions relating C_{GS}, g_m, and ω_T are stated in (3.55) and (3.56).

$$C_{GS} = \frac{2}{3}C_{OX}WL = \frac{2}{3}C_{OX}\frac{W}{L}L^2 = \frac{4}{3}\frac{L^2}{\mu}\frac{I_{DQ}}{V_{EB}^2} \tag{3.55}$$

$$g_m = \mu C_{OX}\frac{W}{L}V_{EB} = \sqrt{2\mu C_{ox}\frac{W}{L}I_{DQ}} = \frac{2I_{DQ}}{V_{EB}} \tag{3.56}$$

The transition frequency of the transistor, ω_T, is the frequency where the short-circuit current gain drops to unity and for a MOS transistor is the ratio of the transconductance gain to the gate-source capacitance. This can be expressed as

$$\omega_T = \frac{g_m}{C_{GS}} = \frac{3}{2}\frac{\mu V_{EB}}{L^2} \tag{3.57}$$

Then,

$$\frac{C_1}{g_{m1}} = \frac{C_{GS1}+C_{GS2}}{g_{m1}} = \frac{\left(\frac{2}{3}\frac{L_1^2}{\mu_n V_{EB1}}\right)\frac{1}{V_{EB1}} + \left(\frac{2}{3}\frac{L_2^2}{\mu_n V_{EB2}}\right)\frac{M}{V_{EB2}}}{\frac{1}{V_{EB1}}} = \frac{1}{\omega_{T1}} + \frac{1}{\omega_{T2}}\frac{MV_{EB1}}{V_{EB2}} \tag{3.58}$$

$$\frac{C_2}{g_{m4}} = \frac{C_{GS3}+C_{GS4}}{g_{m4}} = \frac{\left(\frac{2}{3}\frac{L_3^2}{\mu_p V_{EB3}}\right)\frac{1}{V_{EB3}} + \left(\frac{2}{3}\frac{L_4^2}{\mu_p V_{EB4}}\right)\frac{M}{V_{EB4}}}{\frac{M}{V_{EB4}}} = \frac{1}{\omega_{T3}}\frac{1}{M} + \frac{1}{\omega_{T4}} \tag{3.59}$$

Substituting (3.51), (3.52), (3.58) and (3.59) into (3.48) yields

$$v_1 = \left[\frac{I_{N1}+I_{N3}+\left(s\left(\frac{1}{M\omega_{T3}}+\frac{1}{\omega_{T4}}\right)+\frac{1}{M}\right)\left[I_{N2}+I_{N4}\right]}{\left[s\left(\frac{1}{\omega_{T1}}+\frac{1}{\omega_{T2}}\frac{MV_{EB1}}{V_{EB2}}\right)+\frac{MV_{EB1}}{V_{EB2}}\right]\left[s\left(\frac{1}{M\omega_{T3}}+\frac{1}{\omega_{T4}}\right)+\frac{1}{M}\right]-1}\right]\left[\frac{V_{DD}(M+1)}{2P}V_{EB1}\right] \tag{3.60}$$

Although this expression may appear more complicated than (3.48), it provides more insight into how the design parameters affect the noise performance. In the multi-VT temperature sensor of Figure 3-11, there are 8 degrees freedom that affect the noise performance, $\{W_1, W_2, W_3, W_4, L_1, L_2, L_3, L_4\}$. In (3.60), the noise performance is alternately expressed in terms of the more convenient parameters $\{V_{EB1}, V_{EB2}, M, P, \omega_{T1}, \omega_{T2}, \omega_{T3}, \omega_{T4},\}$.

Given a circuit that is comprised of k transistors, the power spectral density of the output voltage can be expressed as

$$S_P = \sum_{i=1}^{k} \left| T_i(j\omega) \right|^2 S_{Pi} \tag{3.61}$$

where T_i is the transfer function from the i^{th} noise current source to the voltage output and S_{Pi} is the power spectral density of the i^{th} noise current source.

Following the notation used in equation (3.61), the term multiplying each noise current is the transfer function from that current source to the output $\boldsymbol{v}_1$. Denoting the transfer function from the k^{th} noise source to $\boldsymbol{v}_1$ as $T_{k1}(s)$, it follows that these transfer functions can be expressed as:

$$T_{11}(s) = T_{31}(s) = \frac{V_{DD}(M+1)}{2P} \frac{V_{EB1}}{\left[s\left(\frac{1}{\omega_{T1}} + \frac{1}{\omega_{T2}} \frac{MV_{EB1}}{V_{EB2}} \right) + \frac{MV_{EB1}}{V_{EB2}} \right] \left[s\left(\frac{1}{M\omega_{T3}} + \frac{1}{\omega_{T4}} \right) + \frac{1}{M} \right] - 1} \tag{3.62}$$

$$T_{21}(s) = T_{41}(s) = \frac{V_{DD}(M+1)}{2P} \frac{V_{EB1}\left(s\left(\frac{1}{M\omega_{T3}} + \frac{1}{\omega_{T4}} \right) + \frac{1}{M} \right)}{\left[s\left(\frac{1}{\omega_{T1}} + \frac{1}{\omega_{T2}} \frac{MV_{EB1}}{V_{EB2}} \right) + \frac{MV_{EB1}}{V_{EB2}} \right] \left[s\left(\frac{1}{M\omega_{T3}} + \frac{1}{\omega_{T4}} \right) + \frac{1}{M} \right] - 1} \tag{3.63}$$

Rewriting terms

$$T_{11}(s) = T_{31}(s) = \frac{V_{DD}(M+1)}{2P} \frac{V_{EB1}}{s^2 \left(\frac{1}{\omega_{T1}} + \frac{1}{\omega_{T2}} \frac{MV_{EB1}}{V_{EB2}} \right) \left(\frac{1}{M\omega_{T3}} + \frac{1}{\omega_{T4}} \right) + s\left[\left(\frac{1}{M\omega_{T3}} + \frac{1}{\omega_{T4}} \right) \frac{MV_{EB1}}{V_{EB2}} + \left(\frac{1}{\omega_{T1}} + \frac{1}{\omega_{T2}} \frac{MV_{EB1}}{V_{EB2}} \right) \frac{1}{M} \right] + \frac{V_{EB1}}{V_{EB2}} - 1} \tag{3.64}$$

$$T_{21}(s)=T_{41}(s)=\frac{V_{DD}(M+1)}{2P}\frac{V_{EB1}\left(s\left(\frac{1}{M\omega_{T3}}+\frac{1}{\omega_{T4}}\right)+\frac{1}{M}\right)}{s^2\left(\frac{1}{\omega_{T1}}+\frac{1}{\omega_{T2}}\frac{MV_{EB1}}{V_{EB2}}\right)\left(\frac{1}{M\omega_{T3}}+\frac{1}{\omega_{T4}}\right)+s\left[\left(\frac{1}{M\omega_{T3}}+\frac{1}{\omega_{T4}}\right)\frac{MV_{EB1}}{V_{EB2}}+\left(\frac{1}{\omega_{T1}}+\frac{1}{\omega_{T2}}\frac{MV_{EB1}}{V_{EB2}}\right)\frac{1}{M}\right]+\frac{V_{EB1}}{V_{EB2}}-1} \quad (3.65)$$

It can be observed that all transfer functions have a low-pass characteristic. Though these transfer functions all have the same denominator polynomial, evaluation of the transfer functions depends upon four values of ω_T which may differ from one design to the next.

In an attempt to simplify the transfer functions a bit, a new approximate transfer function $\hat{T}_{k1}(s)$ is defined for each of the transfer functions $T_{k1}(s)$ by setting $\omega_{T1}=\omega_{T2}=\omega_{T3}=\omega_{T4}=\omega_T$ in each of these transfer functions. If the ω_{Tk} values are close to each other and if ω_T is selected so that it is close to these values as well, then the approximate transfer functions $\hat{T}_{k1}(s)$ will not differ significantly from $T_{k1}(s)$. If there are appreciable differences in the ω_T values, then the approximate transfer functions will differ somewhat from the actual transfer functions. In the next section, the value of ω_T will be set to be the maximum of $\{\omega_{T1},\omega_{T2},\omega_{T3},\omega_{T4}\}$. The rationale of this selection of ω_T is that the flicker noise will be modestly over estimated. It thus follows by substituting $s=j\omega$ into (3.64) and (3.65), that the following complex expressions are obtained:

$$\hat{T}_{11}(s)\Big|_{s=j\omega}=\hat{T}_{31}(s)\Big|_{s=j\omega}=\frac{V_{DD}(M+1)}{2P}\frac{V_{EB1}}{\frac{V_{EB1}}{V_{EB2}}-1-\left(\frac{\omega}{\omega_T}\right)^2\left(\frac{1+M}{M}+\frac{V_{EB1}(1+M)}{V_{EB2}}\right)+j\frac{\omega}{\omega_T}\left[\frac{V_{EB1}}{V_{EB2}}(2+M)+\frac{1}{M}\right]} \quad (3.66)$$

$$\hat{T}_{21}(s)\Big|_{s=j\omega} = \hat{T}_{41}(s)\Big|_{s=j\omega} = \frac{V_{DD}(1+M)}{2P} \frac{V_{EB1}\left(\frac{1}{M} + j\frac{\omega}{\omega_T}\left(\frac{1+M}{M}\right)\right)}{\frac{V_{EB1}}{V_{EB2}} - 1 - \left(\frac{\omega}{\omega_T}\right)^2\left(\frac{1+M}{M} + \frac{V_{EB1}(1+M)}{V_{EB2}}\right) + j\frac{\omega}{\omega_T}\left[\frac{V_{EB1}}{V_{EB2}}(2+M) + \frac{1}{M}\right]} \quad (3.67)$$

Assuming all noise sources are independent (no correlation with each other), it now follows from (3.61) that the spectral density of the output voltage is given by the expression:

$$S_{OUT1} = \left|T_1(j\omega)\right|^2 S_1 + \left|T_2(j\omega)\right|^2 S_2 + \left|T_3(j\omega)\right|^2 S_3 + \left|T_4(j\omega)\right|^2 S_4 \quad (3.68)$$

And, the spectral density at the output can be approximated by the expression

$$\hat{S}_{OUT1} = \left|\hat{T}_{11}(j\omega)\right|^2 S_1 + \left|\hat{T}_{21}(j\omega)\right|^2 S_2 + \left|\hat{T}_{31}(j\omega)\right|^2 S_3 + \left|\hat{T}_{41}(j\omega)\right|^2 S_4 \quad (3.69)$$

The product of the transfer function magnitude squared and the corresponding noise spectral density represents the output-referred contribution due to each of the noise sources. For notational convenience, the output referred contribution to the spectral density due to each noise source will be denoted as S_{k1} and the approximate spectral densities as $\hat{S}_{k1}$. With this notation, it follows from (3.61) that the output spectral density is given by

$$S_{OUT1} = \sum_{k=1}^{4} S_{k1} \quad (3.70)$$

and the approximate spectral density is given by

$$\hat{S}_{OUT1} = \sum_{k=1}^{4} \hat{S}_{k1} \quad (3.71)$$

The approximate terms $\hat{S}_{11}, \hat{S}_{21}, \hat{S}_{31}, \hat{S}_{41}$ are given by

$$\hat{S}_{11} = \left|\hat{T}_1(j\omega)\right|^2 S_1 = \frac{\left[\frac{V_{DD}(M+1)}{2P}V_{EB1}\right]^2}{\left[\frac{V_{EB1}}{V_{EB2}} - 1 - \left(\frac{\omega}{\omega_T}\right)^2\left(\frac{1+M}{M} + \frac{V_{EB1}(1+M)}{V_{EB2}}\right)\right]^2 + \left[\left(\frac{\omega}{\omega_T}\right)\left(\frac{V_{EB1}}{V_{EB2}}(2+M) + \frac{1}{M}\right)\right]^2} S_1 \tag{3.72}$$

$$\hat{S}_{12} = \left|\hat{T}_2(j\omega)\right|^2 S_2 = \frac{\left[\frac{V_{DD}(M+1)}{2P}V_{EB1}\right]^2\left[\left(\frac{1}{M}\right)^2 + \left(\frac{\omega}{\omega_T}\left(\frac{1+M}{M}\right)\right)^2\right]}{\left[\frac{V_{EB1}}{V_{EB2}} - 1 - \left(\frac{\omega}{\omega_T}\right)^2\left(\frac{1+M}{M} + \frac{V_{EB1}(1+M)}{V_{EB2}}\right)\right]^2 + \left[\left(\frac{\omega}{\omega_T}\right)\left(\frac{V_{EB1}}{V_{EB2}}(2+M) + \frac{1}{M}\right)\right]^2} S_2 \tag{3.73}$$

$$\hat{S}_{13} = \left|\hat{T}_3(j\omega)\right|^2 S_3 = \frac{\left[\frac{V_{DD}(M+1)}{2P}V_{EB1}\right]^2}{\left[\frac{V_{EB1}}{V_{EB2}} - 1 - \left(\frac{\omega}{\omega_T}\right)^2\left(\frac{1+M}{M} + \frac{V_{EB1}(1+M)}{V_{EB2}}\right)\right]^2 + \left[\left(\frac{\omega}{\omega_T}\right)\left(\frac{V_{EB1}}{V_{EB2}}(2+M) + \frac{1}{M}\right)\right]^2} S_3 \tag{3.74}$$

$$\hat{S}_{14} = \left|\hat{T}_4(j\omega)\right|^2 S_4 = \frac{\left[\frac{V_{DD}(M+1)}{2P}V_{EB1}\right]^2\left[\left(\frac{1}{M}\right)^2 + \left(\frac{\omega}{\omega_T}\left(\frac{1+M}{M}\right)\right)^2\right]}{\left[\frac{V_{EB1}}{V_{EB2}} - 1 - \left(\frac{\omega}{\omega_T}\right)^2\left(\frac{1+M}{M} + \frac{V_{EB1}(1+M)}{V_{EB2}}\right)\right]^2 + \left[\left(\frac{\omega}{\omega_T}\right)\left(\frac{V_{EB1}}{V_{EB2}}(2+M) + \frac{1}{M}\right)\right]^2} S_4 \tag{3.75}$$

Up to this point, the spectral densities have been expressed in terms of the excess bias voltages, P, ω_T, and M. For analytical purposes, it may also be useful to express the spectral densities in terms of the actual design variables. The relationship between the excess bias voltages and the W/L ratios is

$$\frac{V_{EB1}}{V_{EB2}} = \sqrt{\frac{W_2 L_1}{M W_1 L_2}} \tag{3.76}$$

Thus, in terms of the W/L ratios, M and P, the spectral densities of (3.72) – (3.75) can be expressed equivalently as:

$$\hat{S}_{11}=\frac{\left(\frac{L_1}{2\mu_n C_{ox}W_1}\right)\left(\frac{V_{DD}}{P}(1+M)\right)}{\left[\sqrt{\frac{W_2L_1}{MW_1L_2}}-1-\left(\frac{\omega}{\omega_T}\right)^2\left(\frac{1+M}{M}+\sqrt{\frac{W_2L_1}{MW_1L_2}}(1+M)\right)\right]^2+\left[\left(\frac{\omega}{\omega_T}\right)\left(\sqrt{\frac{W_2L_1}{MW_1L_2}}(2+M)+\frac{1}{M}\right)\right]^2}S_1 \tag{3.77}$$

$$\hat{S}_{12}=\frac{\left(\frac{L_1}{2\mu_n C_{ox}W_1}\right)\left(\frac{V_{DD}}{P}(1+M)\right)\left[\left(\frac{1}{M}\right)^2+\left(\frac{\omega}{\omega_T}\left(\frac{1+M}{M}\right)\right)^2\right]}{\left[\sqrt{\frac{W_2L_1}{MW_1L_2}}-1-\left(\frac{\omega}{\omega_T}\right)^2\left(\frac{1+M}{M}+\sqrt{\frac{W_2L_1}{MW_1L_2}}(1+M)\right)\right]^2+\left[\left(\frac{\omega}{\omega_T}\right)\left(\sqrt{\frac{W_2L_1}{MW_1L_2}}(2+M)+\frac{1}{M}\right)\right]^2}S_2 \tag{3.78}$$

$$\hat{S}_{13}=\frac{\left(\frac{L_1}{2\mu_n C_{ox}W_1}\right)\left(\frac{V_{DD}}{P}(1+M)\right)}{\left[\sqrt{\frac{W_2L_1}{MW_1L_2}}-1-\left(\frac{\omega}{\omega_T}\right)^2\left(\frac{1+M}{M}+\sqrt{\frac{W_2L_1}{MW_1L_2}}(1+M)\right)\right]^2+\left[\left(\frac{\omega}{\omega_T}\right)\left(\sqrt{\frac{W_2L_1}{MW_1L_2}}(2+M)+\frac{1}{M}\right)\right]^2}S_3 \tag{3.79}$$

$$\hat{S}_{14}=\frac{\left(\frac{L_1}{2\mu_n C_{ox}W_1}\right)\left(\frac{V_{DD}}{P}(1+M)\right)\left[\left(\frac{1}{M}\right)^2+\left(\frac{\omega}{\omega_T}\left(\frac{1+M}{M}\right)\right)^2\right]}{\left[\sqrt{\frac{W_2L_1}{MW_1L_2}}-1-\left(\frac{\omega}{\omega_T}\right)^2\left(\frac{1+M}{M}+\sqrt{\frac{W_2L_1}{MW_1L_2}}(1+M)\right)\right]^2+\left[\left(\frac{\omega}{\omega_T}\right)\left(\sqrt{\frac{W_2L_1}{MW_1L_2}}(2+M)+\frac{1}{M}\right)\right]^2}S_4 \tag{3.80}$$

These expressions are then used to predict the noise performance of the circuit by evaluating the design parameters. We will now bring to closure this noise analysis in the context of the multi-VT temperature sensor. From (3.61), the spectral density of the output can be expressed as

$$S_{OUT1} = \sum_{i=1}^{4} \left| T_i(j\omega) \right|^2 S_i \tag{3.81}$$

and the approximate spectral density at the output is given by

$$\hat{S}_{OUT1} = \sum_{i=1}^{4} \hat{S}_{i1} \tag{3.82}$$

From the derivations in Appendix 2B (2.58), (2.64), and (2.65), the RMS noise temperature is given by

$$T_{[f_{START},\infty]} = \frac{1}{\gamma} \sqrt{\int_{f_{START}}^{\infty} \left[\sum_{i=1}^{4} \left(\left| T_{i1}(j\omega) \right|^2 S_i \right) \right] df} \tag{3.83}$$

From an extension of (2.54) and (2.55), the flicker and white RMS noise temperatures can be approximately expressed as

$$T_{RMS-Flicker[f_{START},\infty]} \simeq \frac{1}{\gamma} \sqrt{\int_{f_{START}}^{f_{NCH}} \left[\sum_{i=1}^{4} \left(\left| T_{i1}(j\omega) \right|^2 \frac{K_{Fi} I_{Di}^{AFi}}{C_{OX} L_{effi}^2 f^{EFFi}} \right) \right] df} \tag{3.84}$$

$$T_{RMS-Thermal[f_{START},\infty]} \simeq \frac{1}{\gamma} \sqrt{\int_{f_{START}}^{f_{NCL}} \left[\sum_{i=1}^{4} \left(\left| T_{i1}(j\omega) \right|^2 \frac{8}{3} kTg_{mi} \right) \right] df} \tag{3.85}$$

where f_{NCH} is the highest of the noise corner frequencies and where f_{NCL} is the lowest of the noise corner frequencies.

Since the pole frequencies of the transfer functions are typically somewhat higher than the noise corner frequencies, the lowpass transfer functions do not differ much from their dc values so the flicker noise temperature can be expressed as

$$T_{RMS-Flicker[f_{START},\infty]} \simeq \frac{1}{\gamma}\sqrt{\int_{f_{START}}^{f_{NCH}}\left[\sum_{i=1}^{4}\left(\left|T_{i1}(j0)\right|^2 \frac{K_{Fi} I_{Di}^{AFi}}{C_{OX} L_{effi}^2 f^{EFFi}}\right)\right]df} \quad (3.86)$$

Finally, the expressions in (3.83) – (3.86) can be simplified somewhat by replacing the transfer functions $T_{k1}(j\omega)$ with the approximate transfer functions $\hat{T}_{k1}(j\omega)$.

ANALYTICAL AND SIMULATION RESULTS OF MULTI-VT 4T TEMPERATURE SENSOR

The multi-VT 4T temperature sensor in Chapter 3 is used for the noise analysis. The device sizes are shown in Table 3-2.

Table 3-2: Transistors size for P-type reverse Widlar temperature sensor

Transistor	M_1	M_2	M_3	M_4
Size (μm)	$\frac{W_1}{L_1}=\frac{2\times0.15}{1}$	$\frac{W_2}{L_2}=\frac{6\times0.8}{1}$	$\frac{W_3}{L_3}=\frac{10\times0.15}{1}$	$\frac{W_4}{L_4}=\frac{10\times0.15}{1}$

The analytical noise expression is evaluated and compared with the simulation output from Cadence SPICE. In the analytical analysis, the transfer function approximation was used where $\omega_T = \max\{\omega_{T1}, \omega_{T2}, \omega_{T3}, \omega_{T4}\}$ where $\omega_T = 2\pi f_T$. In this design, the values for these parameters were $f_{T1} = 1.14\ GHz$, $f_{T2} = 363\ MHz, f_{T3} = 338\ MHz$ and $f_{T4} = 340\ MHz$.

The frequency domain noise output is shown in Figure 3-16.

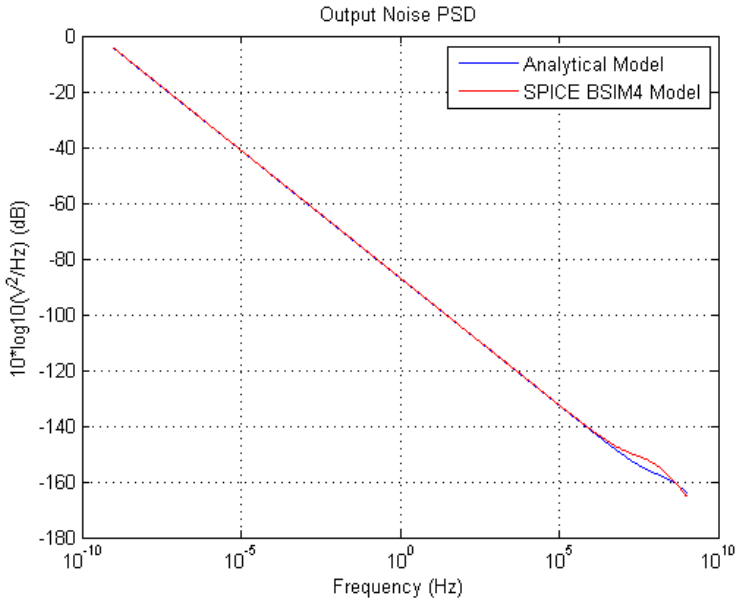


Figure 3-16: Output noise power spectral density for multi-VT 4T temperature sensor

From this analysis, it can be observed that the analytical approximations agree closely with the simulation results throughout the flicker noise region. There is a modest difference in the thermal noise region but in this structure, the noise performance is dominated by the flicker noise.

The time-domain RMS noise temperature was obtained for different operating times, T_{OPP}, by taking the integral given in (3.83) of the output noise PSD from $f_{START} = 1/T_{OPP}$ to 10MHz. The parameter γ for this design was $\gamma = 0.77 mV/K$. The integral was stopped at 10MHz because the total noise contribution at higher frequencies is negligible since the filter rolls of the high-frequency thermal noise contributions above 10MHz. Specifically, this integral was

$$T_{\left[1/T_{OPP},\,10MHz\right]} = \frac{1}{\gamma}\sqrt{\int_{1/T_{OPP}}^{10\,MHz}\left[\sum_{i=1}^{4}\left(\left|T_{i1}(j\omega)\right|^2 S_i\right)\right]df} \qquad (3.87)$$

The time-domain noise performance plot is then obtained by taking the integral of the output noise PSD from 10MHz to range of frequencies corresponding to the equivalent time periods. The results are shown in Figure 3-17.

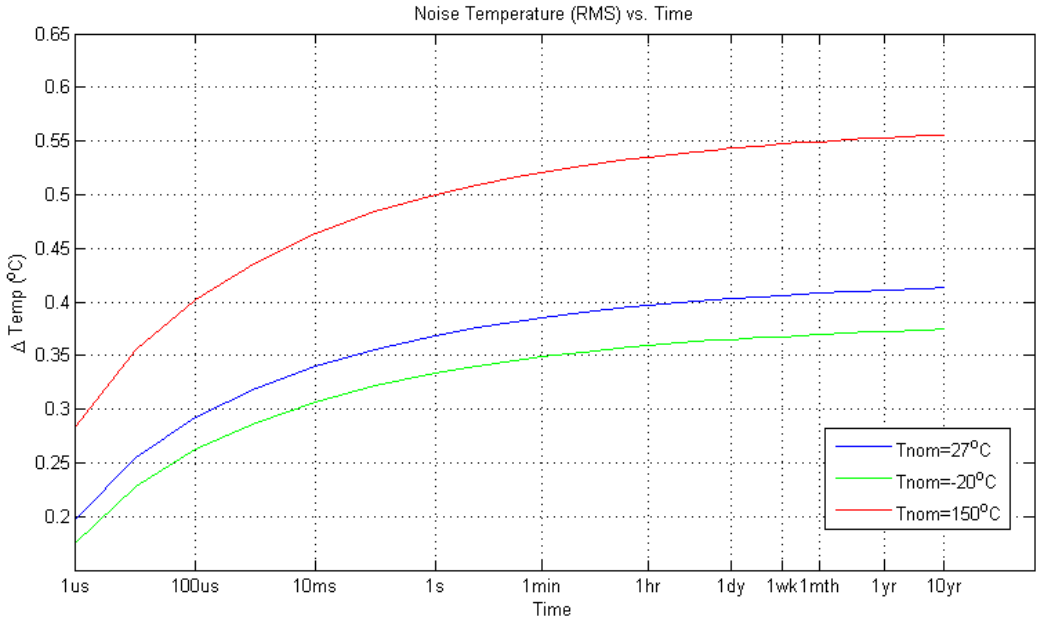


Figure 3-17: RMS noise temperature of the multi-VT 4T temperature sensor in time domain

From the plots, it can be inferred that this implementation of the multi-VT 4T temperature sensor will have a RMS noise temperature of 0.56°C over the period of 10 years. This shows that the flicker noise is quite high for small feature size process and can significantly affect the temperature sensing performance (56% of 1°C error). Hence, the transistors sizes cannot be too small if good accuracy is required and trade-offs between area and accuracy must be a part of the design strategy. There are methods for mitigating the 1/f noise degradation with small device areas but they will not be discussed here.

CHAPTER 4 FULL DESIGN OF CASCODE MULTI-VT THRESHOLD BASED TEMPERATURE SENSOR

4.1 INTRODUCTION

Following the analysis from previous chapter, a full design example of a cascode multi-VT threshold based temperature sensor is presented. The temperature sensor has been designed to operate in the temperature range from -20°C to 100°C. The circuit is implemented in a digital 65nm process with multiple threshold devices. The nominal supply voltage is 1.2V. Simulation results portraying the analog output voltage and temperature nonlinearity errors (INL) across the specified temperature range, noise performance, and the cascode self-biasing DC loop test (appendix) are presented.

4.2 DESIGN OF A CASCODE TEMPERATURE SENSOR

Using the same design strategy as in the previous chapter, a 4-transistors multi-VT cell is first designed. The initial goal is to obtain a stable operating point with all transistors operating in saturation – strong inversion, as well as to reach reasonable temperature sensing performance with a temperature INL that is less than 1°C. Then, wide-swing cascoding is used to decrease the supply sensitivity. The fully-cascoded multiple-VT temperature sensor is shown in Figure 4-1.

The cascode transistors are sized to be slightly larger than the basic 4-transistors cell to provide optimum voltage headroom. This is because for a fixed quiescent current level,

increasing the W/L ratio will decrease the excess-bias voltage, V_{EB}, and thus reducing drain-source voltage, V_{DSAT}.

The cascode transistors themselves are self-biased by bootstrapping off of the output nodes of the core sensor itself. The self-biasing circuit is also shown in Figure 4-1. Bootstrapping of the bias generator introduces additional coupled feedback loops in the circuit as can be observed from the circuit of Figure 4-1. Since additional feedback loops are formed, it is necessary to determine if additional stable equilibrium points are created so that startup circuits can be added, if needed.

A systematic method for determining all possible operating points for the circuit is needed to determine if the circuit has multiple stable equilibrium points. The problem of considering the coupled feedback loops could be avoided by biasing the cascode transistors with external bias generators but there appear to be benefits from both device count and a power dissipation viewpoint to use the self-bias approach. A theoretical investigation of the equilibrium points for this structure based upon the “contraction principle” is discussed in Appendix 4. In this investigation, a process is established for determining whether any specific implementation of this circuit has multiple equilibrium points. This process requires a computer simulation for each implementation. It is conjectured that start-up circuits are not needed for this self-biased structure but at this stage it can only be observed that all implementations that were considered do not require startup circuits.

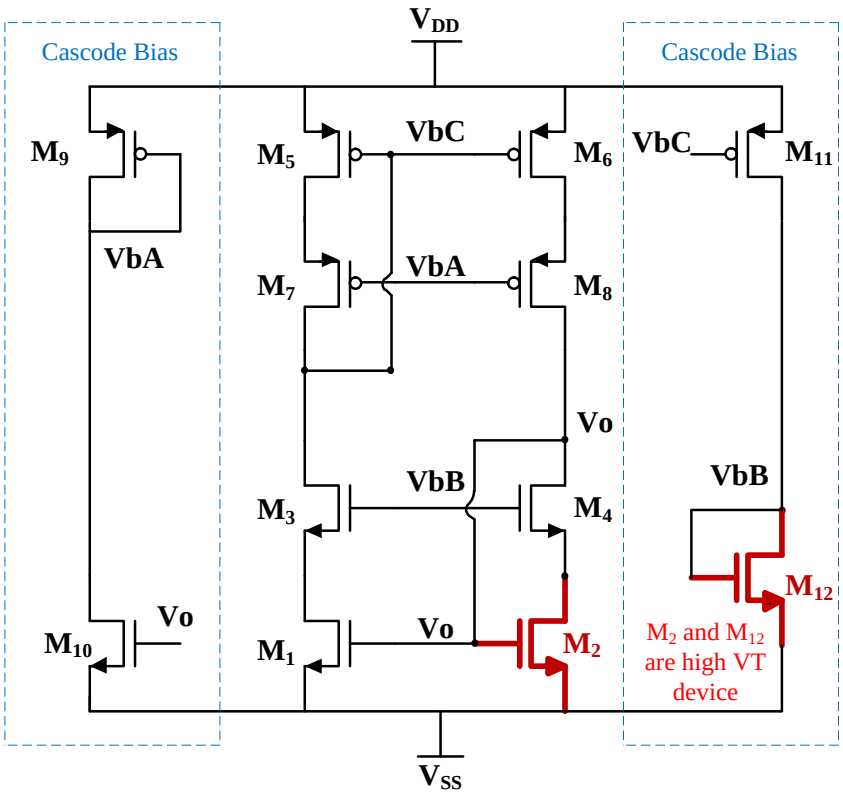


Figure 4-1: Schematic of cascode temperature sensor with biasing transistors

Table 4-1: Transistors size and type for cascode temperature sensor

Transistor	Size (µm)	Type
M1	$W_1/L_1 = 2\times0.15/1.5$	Nominal 1.2V NMOS
M2	$W_2/L_2 = 4\times0.8/1.6$	High-VG 1.2V NMOS
M3	$W_3/L_3 = 4\times2\times0.15/1$	Nominal 1.2V NMOS
M4	$W_4/L_4 = 4\times2\times0.15/1$	Nominal 1.2V NMOS
M5	$W_5/L_5 = 4\times4\times0.15/1$	Nominal 1.2V PMOS
M6	$W_6/L_6 = 4\times4\times0.15/1$	Nominal 1.2V PMOS
M7	$W_7/L_7 = 5\times4\times0.15/1$	Nominal 1.2V PMOS
M8	$W_8/L_8 = 5\times4\times0.15/1$	Nominal 1.2V PMOS
M9	$W_9/L_9 = 0.15/0.6$	Nominal 1.2V PMOS
M10	$W_{10}/L_{10} = 0.15/1$	Nominal 1.2V NMOS
M11	$W_{11}/L_{11} = 2\times4\times0.15/0.5$	Nominal 1.2V PMOS
M12	$W_{12}/L_{12} = 0.8/6$	High-VG 1.2V NMOS

An implementation of this temperature sensor was made in the 65nm process. In this design, the major emphasis was on demonstrating functionality of the temperature sensor rather than focusing on design optimality. The transistor sizes used in this implementation are shown in Table 4-1. Since the threshold voltages decrease with device length, l, long-channel devices were used to keep the threshold voltage low thus preserving headroom. The device sizes are relatively large for a 65nm process. However, this may offer some benefits in noise performance, as discussed in the Appendix 3B.

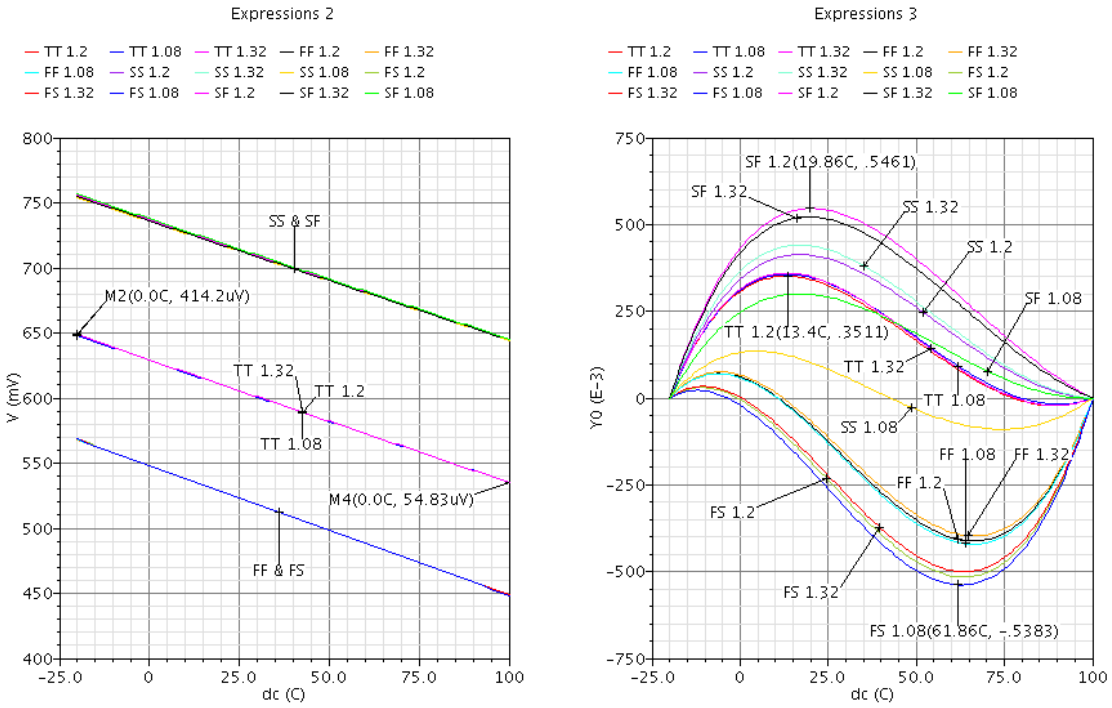
4.3 SIMULATION RESULTS

It is shown by simulation in Appendix 4, using the contraction principle, that this implementation has a single stable equilibrium point and thus does not require a startup circuit.

Simulation results showing the output voltage and the linearity error for TT as well as for the four process corners are shown in Figure 4-2. These simulation results are for three different supply voltages, the nominal supply voltage of 1.2V and for supply voltage variations of ±10% above and below nominal.

At TT, the nominal temperature coefficient is -0.944mV/°C. This temperature coefficient ranges from -1mV/°C to -0.92mV/°C due to process variations at a fixed supply voltage and ranges from -0.943mV/°C to -0.946mV/°C at a fixed process corner (TT) as the supply varies between the high and low values. Over a 120°C operating range, this would correspond to a temperature error of $\Delta T_{process} = \frac{0.08mV}{0.944mV} \bullet \frac{120}{2} = 5.08^{o}C$ and

$\Delta T_{supply} = \frac{0.003mV}{0.944mV} \bullet \frac{120}{2} = 0.19^{o}C$. However, the slope error due to process variations in the slope can be calibrated out with a two-point calibration or significantly reduced with a batch calibration.



(a) (b)

Figure 4-2: Simulated cascode circuit (a) output voltage and (b) temperature error at different process corners and ±10% variation over nominal VDD of 1.2V

Simulation results show a worst-case slope variation with supply variations occurs at SF of $\Delta T = \frac{0.008mV}{0.924mV} \bullet \frac{120}{2} = 0.52^{o}C$ over a 120°C operating range. Although this slope error cannot be calibrated out, it does not cause a significant loss in accuracy.

The simulation results show a variation of approximately 190mV with process variations from FF to SS. Although this would cause an error of approximately

$\frac{190\text{mV}}{0.994\text{mV}/°\text{C}} = 191°\text{C}$ if uncalibrated, this error can be eliminated with a single-point calibration. At TT, the maximum output voltage variation is 0.414mV and with nominal temperature coefficient of -0.944mV/°C, it would cause additional temperature error of 0.44° C if V_{DD} varies ±10% in real-time. This is significantly less than the error that would be experienced without cascoding. Although this error has been reduced, it remains a significant contributor to the overall temperature error budget. More emphasis in the design on reducing this error by a factor of 4, in part in the basic 4-transistor cell, and in part in the cascode circuits, will likely prove effective. If this error can be reduced by a factor of 4, it will not contribute significantly to the overall temperature error budget.

It can be seen from Figure 4-2(b) that the maximum nonlinear error at typical conditions is 0.3511°C across the temperature range between -20°C and 100°C; while the worst-case maximum temperature error occurs at SF corner and low voltage, which is 0.5461°C. The INL performance of this circuit, based upon the models used in the simulator, is quite good.

The simulated noise spectral density of this temperature sensor is shown in Figure 4-3. Since the cascode multi-VT structure composes of all transistors and is designed to operate at DC, 1/f noise is dominant and can introduce significant temperature error. Findings from [**27**] show that deep-submicron processes such as the 65nm digital process can have significantly larger 1/f noise than larger feature size processes such as the 0.18μm process. Hence, for the case of analog design in 65nm digital process, the transistors should be sized optimally large enough to keep the noise level down.

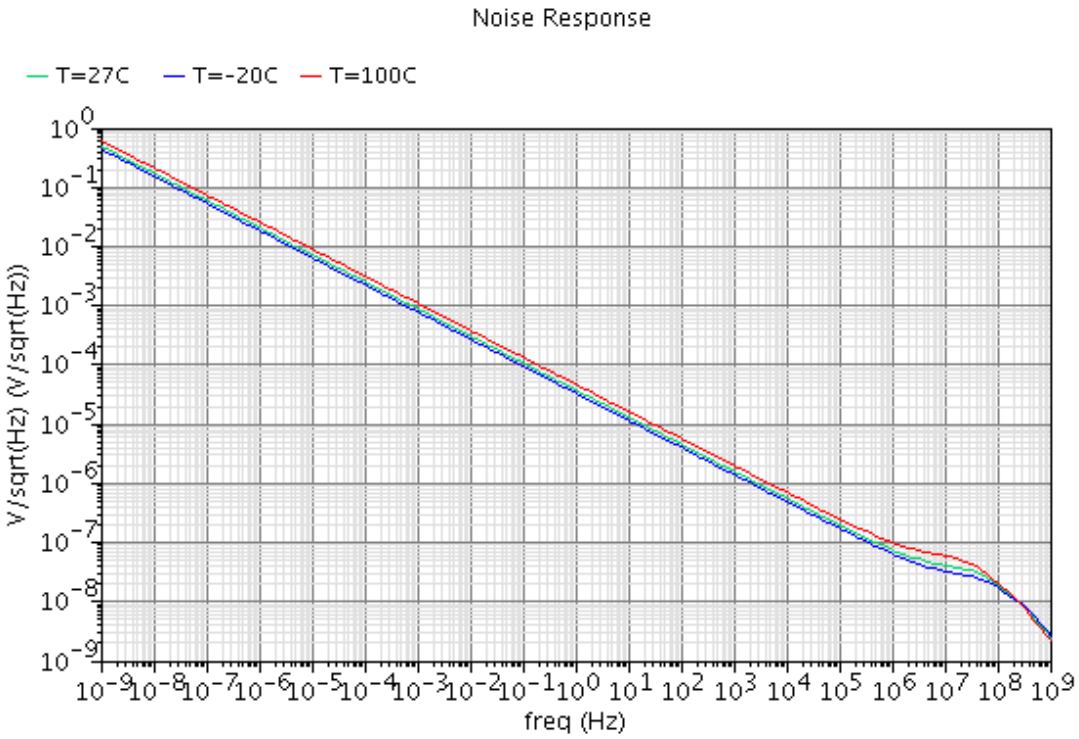


Figure 4-3: Cascode circuit noise simulation in frequency domain for low to high temperature range

Figure 4-4 depicts the noise performance in the time domain. These simulations show that when operating continuously at 100°C for 10 years, the noise in the cascode circuit will contribute a temperature error of approximately 0.4°C RMS. This is also significant contributor to the overall temperature error budget. Some reductions in this error can be obtained by increasing the lengths of the transistors in the sensor.

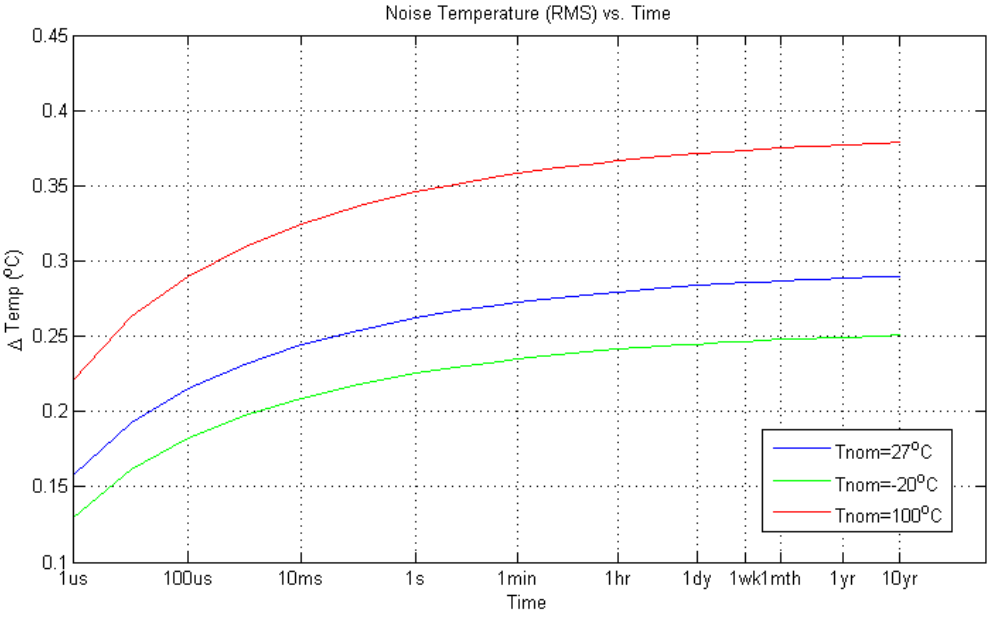


Figure 4-4: Cascode circuit noise simulation in time domain for low to high temperature range

A summary to the overall simulated results appear in Table 4-2. In its current implementation, the area is quite small and the power dissipation is very low.

Table 4-2: Summary of performance for cascode multi-VT temperature sensor

Specification	**Performance**
Process	65nm
Voltage Supply	1.2V
Temperature Range	-20~100˚C
Parameter	**Cascode Multi-VT**
Layout Estimated Area (μm^2)	450
Nominal power consumption (μW)	20.5
Temperature Coefficient (mV/ ˚C)	-0.944
Max. Temp. INL (˚C) at Typical	0.351
Max. Temp. INL (˚C) at Worst Case	0.546
Supply Sensitivity over ±10% Variation at Typical (˚C)	0.44
Max. RMS Noise Temperature (˚C)	0.38

4.3.1 Comparison with recent integrated temperature sensors[1]

Table 4-3: List of published temperature sensors and proposed temperature sensors

Sensors	Max Temperature Error (°C)	Temperature Range (°C)	Supply Sensitivity (°C/V)	Layout Area (mm^2)	Power Consumption (µW)	CMOS Process
Thermal diode, Intel [**5**]	±8	40 – 110	n/a	n/a	n/a	n/a
Thermal diode, AMD [**6**]	±10	-55 – 85	n/a	n/a	10 – 100	90nm
PN junction based, PowerPC [**28**]	±4 with trim	10 – 100	n/a	n/a	n/a	n/a
PN junction based [**29**]	0.1 (1 corner, 3σ)	-55 – 125	0.05	4.5	> 187.5	0.7µm
PN junction based [**30**]	0.2 (trimmed, 3σ)	-70 – 125	1.2	0.1	9.96	65nm
PN junction based [**31**]	<5	-10 – 110	n/a	0.02	1600	32nm
Ring oscillator based [**32**]	~7 (corners)	40 – 150	n/a	n/a (14 transistors)	25	45nm
Ring oscillator based [**33**]	-2.9 – +2.75	-40 – 110	n/a	0.0013	400	65nm
TDC [**24**]	-0.7 – +0.9	0 – 100	n/a	0.175	10	0.35µm
CMOS threshold voltage based [**23**]	-1 – 0.8	50 – 125	n/a	50e-6 (Needs external current mirror)	25	90nm
Previous Work [**17**]	0.05 (TT)	-20 – 100	14.69	2e-4	93.6	0.18µm
P-type 5T	0.052 (TT)	-20 – 100	16.36	3.2e-4	30.6	0.18µm
Master-Slave Hybrid [**18**]	0.2 (TT)	-20 – 100	n/a	0.0108	324 (continuous)	0.18µm
Multi-VT 4T High Temp	0.055 (TT)	100 – 150	49.62	5.4e-5	11.02	65nm
Multi-VT Cascode High Temp	0.177 (TT)	100 – 150	1.36	9.6e-5	5.12	65nm
Multi-VT Cascode Full Range	0.351 (TT)	-20 – 100	1.83	4.5e-4	20.5	65nm

1. Partial data compiled by [**18**]

The key performances parameters of published temperature sensors are compared with the temperature sensors in Table 4-3. It is somewhat difficult to make a fair comparison with other works since most authors do no discuss variations in performance with process, variations in performance with supply voltage, or variations in performance with device noise. It is apparent, at least for the proposed temperature sensors, that these factors can be significant contributors to the overall temperature error budget.

With these qualifications, it can be observed that the proposed circuits have better temperature sensing accuracy compared with current on-die temperature sensors for thermal management in microprocessors [**5**] [**6**] [**28**] as well as temperature sensor of similar type [**23**]. While there is no direct comparison with smart temperature sensors with digital interface [**29**] [**30**] [**31**] [**33**] [**24**] [**18**], the very small area and high temperature linearity of the proposed multi-VT cascode temperature sensor make it very attractive as an analog temperature sensing front-end to be coupled with a temperature-to-digital converters. Self-referencing techniques with successive approximation comparison presented in [**18**] can be adapted to provide digital output for the proposed circuit.

4.4 CONCLUSION

A highly linear, small area, low voltage multi-VT based cascode temperature sensor has been proposed and implemented in a 1.2V 65nm digital process. Exploiting the natively available multiple threshold transistors in the digital process, the proposed circuit manages has ample voltage headroom for low supply voltage operation as well as cascoding to significantly reduce the output voltage sensitivity due to supply variation. In addition, since the proposed circuit only uses transistors operating in saturation and that it is simply two-inverters in a loop, it can be easily implemented in small feature size digital process with low supply voltages. Given more time and effort, the proposed circuit can be further optimized to reduce power consumption and area without worsening the temperature sensing and noise performance.

APPENDIX 4 CASCODE SELF-BIASING DC LOOP TEST

The proposed cascode multi-VT threshold extraction circuit employs a self-biasing scheme to generate the bias voltages for both of the n-channel and p-channel cascode transistor pairs. The output node of the bottom n-channel transistor pair is mirrored out to bias the p-channel cascode transistor pair; while the output node of the top p-channel transistors pair is mirrored out to bias the n-channel cascode transistor pair.

Although it has been shown that the basic 4-transistor multi-VT cell has one stable equilibrium point, the self-basing loops introduced in the cascode version of the circuit raise concerns about whether the overall circuit has multiple stable equilibrium points. The concerns about multiple stable equilibrium points in the temperature sensors have been addressed in Chapters 2, 3, and 4 where the temperature sensor circuits all have a single feedback loop. In the analog circuit design community, there is an awareness that multiple stable equilibrium points in circuits with a feedback loop may exist and circuit modifications that are typically termed “start-up circuits” are regularly used to eliminate undesired stable equilibrium points if they exist. But though there is awareness, there is little if any formal discussion in the literature about how to actually determine if a start-up circuit is needed and ad hoc solutions are invariably used to address these problems. The concept of breaking the feedback loop and observing the number of intersection points of the loop gain with the unity loop gain line that was discussed in previous chapters of this thesis is one of the first formal approaches to addressing the issue of multiple stable equilibrium points in the analog design community. In the circuits considered in this thesis, the loop was broken at a point where the dc input impedance to the open-loop structure was infinite and this eliminated errors that

would be introduced if the dc loading was perturbed by breaking the loop. But a direct extension of this approach to arbitrary circuits that have two or more feedback loops does not appear to be straightforward.

The issue of potentially multiple stable equilibrium points in nonlinear systems with multiple feedback loops has been formally addressed by the nonlinear control systems community. A well-known method for determining whether such a system has a single stable equilibrium point is based upon the contraction mapping. In this appendix the contraction mapping approach will be adapted to nonlinear analog circuits that have two or more feedback loops.

CONTRACTION MAPPING PRINCIPLE

The contraction approach is based upon a Mathematical theorem proposed by Stefan Banach in 1922, known as the "Banach fixed point theorem" or commonly as the "contraction mapping principle" [**34**]. This theorem, as stated in [**35**], is:

> **Theorem 1.1.** *Let* $(\boldsymbol{X}, d)$ *be a complete metric space and* $f: \boldsymbol{X} \to \boldsymbol{X}$ *be a map such that* $d\big(f(x), f(x')\big) \leq cd(x, x')$ *for some* $0 \leq c < 1$ *and all* x *and* x' *in* $\boldsymbol{X}$. *Then* f *has a unique fixed point in* $\boldsymbol{X}$. *Moreover, for any* $x_0 \in \boldsymbol{X}$ *the sequence of iterates* $x_0, f(x_0), f\big(f(x_0)\big), \ldots$ *converges to the fixed point of* f.
>
> *When* $d\big(f(x), f(x')\big) \leq cd(x, x')$ *for some* $0 \leq c < 1$ *and all* x *and* x' *in* $\boldsymbol{X}$, f *is called a contraction. A contraction shrinks distances by a uniform factor c less than 1 for all pairs.*

With this notation, the theorem can be more succinctly stated as

Theorem Let $(\boldsymbol{X}, d)$ be a complete metric space and $f: \boldsymbol{X} \rightarrow \boldsymbol{X}$ be a contraction mapping. Then f has a unique fixed point, x_F, in $\boldsymbol{X}$ and for any $x_0 \in \mathbf{X}$ the sequence of iterates $x_0, f(x_0), f\big(f(x_0)\big), \ldots$ converges to x_F.

CIRCUIT LOOP ANALYSIS

The self-biased fully cascoded temperature sensor is repeated in Figure 4-5. The nodes VbC and Vo have been marked with "X". All feedback loops can be broken by making breaks at these two nodes and this is the minimal number of break nodes that are required to break all feedback loops.

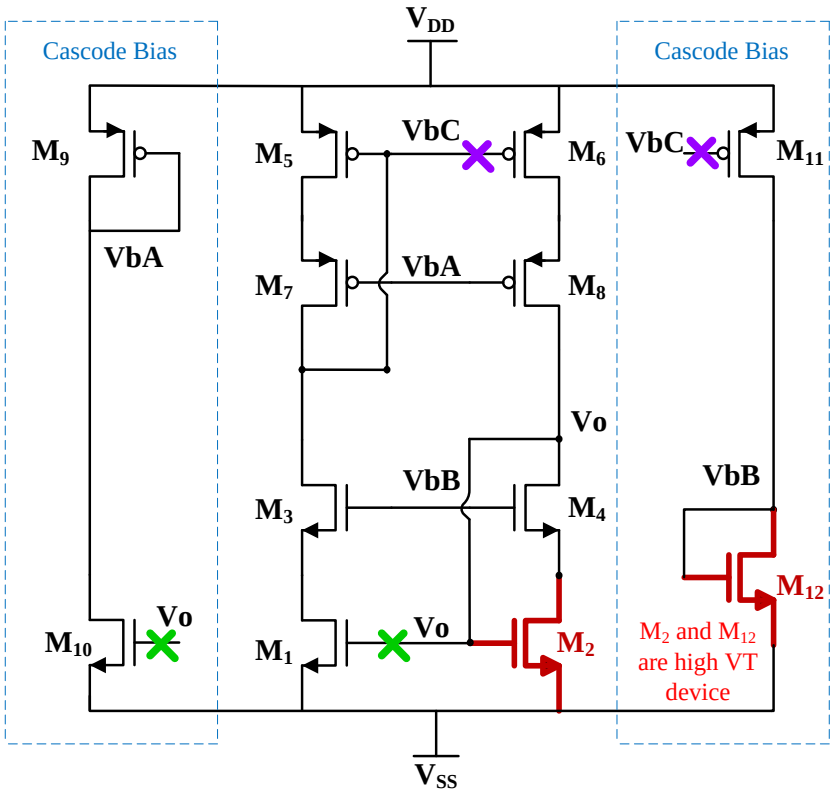


Figure 4-5: Full cascoded temperature sensor of Figure 4-1

After breaking the loops at two nodes, we can designate an input and an output voltage at each of the broken nodes. These are denoted by the pairs (V_{oP}, V_{iP}) and (V_o, V_i) as shown in Figure 4-6. Of course, during normal operation we have V_{oP}=V_{iP} and V_o=V_i. Note that by breaking the loops at these two nodes, the dc input impedances seen at both V_{iP} and V_i are ideally infinite. Thus breaking the loop does not alter the loading on the output nodes V_{oP} and V_o.

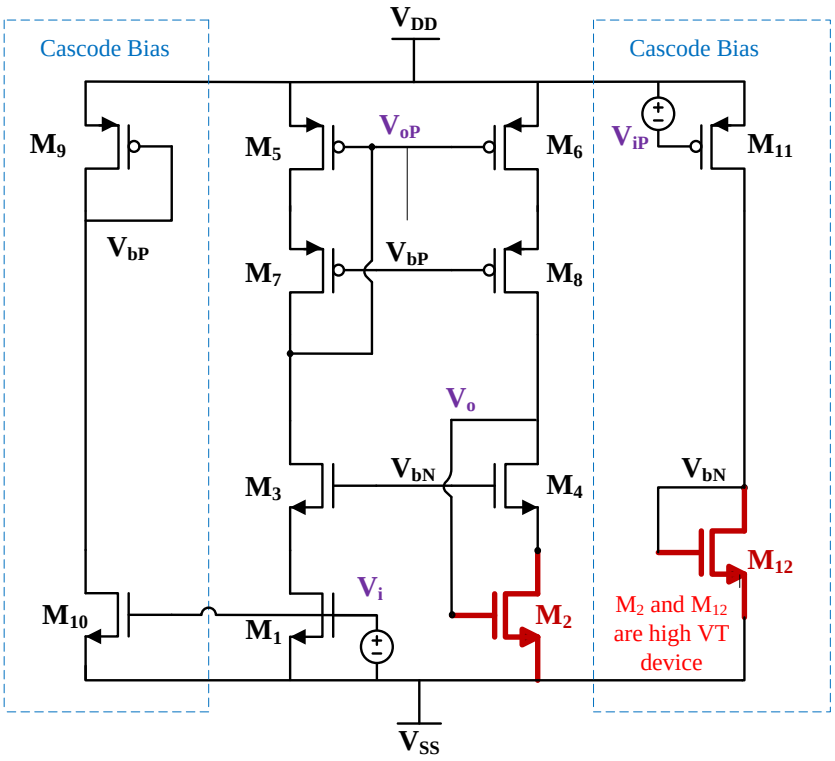


Figure 4-6: Fully cascoded temperature Sensor with all feedback loops broken

Define the relationship between the inputs and outputs in this nonlinear circuit by the function f and designated as $\begin{pmatrix} V_o \\ V_{oP} \end{pmatrix} = f\begin{pmatrix} V_i \\ V_{iP} \end{pmatrix}$. The function f is a mapping $f: \boldsymbol{V} \to \boldsymbol{V}$ where $\boldsymbol{V} \in \mathbb{R}^2$. Thus the function f defines a mapping from the metric space $\mathbb{R}^2$ onto the metric space $\mathbb{R}^2$ with the metric being the Euclidian metric. In accordance with the Contraction

Mapping Principle stated above, the circuit will have a unique operating point for V_o and V_{oP} if f is a contraction mapping. And, if f is a contraction mapping, then for any initial iterate, the sequence defined by $\begin{pmatrix} V_{i(k+1)} \\ V_{iP(k+1)} \end{pmatrix} = f\begin{pmatrix} V_{i(k)} \\ V_{iP(k)} \end{pmatrix}$ converges to a point designated as $\begin{pmatrix} V_i \\ V_{iP} \end{pmatrix}^*$ and this is the stable equilibrium operating point of the circuit. This can be alternatively and equivalently stated that if f is a contraction mapping, then the circuit will have a single stable equilibrium point.

At this point, I will not prove that f is a contraction mapping. Alternatively, I will develop a contraction process that is suitable for computer simulations that can be used to show that a circuit with multiple feedback loops has a single stable equilibrium point. This process will be based upon a contraction of the input domain that contains all stable equilibrium points with the recognition that if this domain contracts to a single point, than the circuit will have a single stable equilibrium point. This process will be developed specifically to show that the self-biased cascoded temperature sensor with two break points has a single stable equilibrium point but it can be extended to show that circuits that require a single break point or that have multiple break points also have a single stable equilibrium point. This contraction process will provide sufficient but not necessary conditions for showing that a circuit has a single stable equilibrium point.

DOMAIN CONTRACTION MAPPING

Define the two-dimensional rectangular region $\mathbf{R}_0$ to be a region that bounds all possible output voltages for the circuit obtained by breaking all feedback loops as

constrained by the supply voltages for the circuit. Let the set **E** be the set of equilibrium points. **E** is comprised of both the stable and unstable equilibrium points of the circuit. If the circuit has a single stable equilibrium point, the set **E** will contain a single point. Define $\mathbf{A}_0$ to be the region spanned by the output of the circuit for any input in $\mathbf{R}_0$. Define the rectangle $\mathbf{R}_1$ to be a rectangular region that includes $\mathbf{A}_0$ as a subset. Mathematically, $\boldsymbol{A}_0 = f(\boldsymbol{R}_0)$. The region $\mathbf{A}_0$ is a subset of $\mathbf{R}_0$ ($\boldsymbol{A}_0 \subset \boldsymbol{R}_0$) and the rectangle $\mathbf{R}_1$ can be selected so that is also a subset of $\mathbf{R}_0$ ($\boldsymbol{R}_1 \subset \boldsymbol{R}_0$). It can be observed that all equilibrium points are elements of both $\mathbf{R}_0$ and $\mathbf{A}_0$ and hence all equilibrium points are elements of $\mathbf{R}_1$ ($\boldsymbol{E} \subset \boldsymbol{R}_1$). This process can be recursively extended. Define the region $\mathbf{A}_k$ to be the region spanned by the output of the circuit for any input in $\mathbf{R}_k$ and define the rectangle $\mathbf{R}_{k+1}$ to be a rectangular region that includes $\mathbf{A}_k$ as a subset and that is also a subset of $\mathbf{R}_k$. It follows that **E** is also a subset of $\mathbf{R}_{k+1}$. Mathematically, this can be written as

$$\mathbf{A}_k = f(\mathbf{R}_k) \tag{4.1}$$

$$\mathbf{A}_k \subset \mathbf{R}_{k+1} \tag{4.2}$$

$$\mathbf{E} \subset \mathbf{R}_{k+1} \tag{4.3}$$

With this process, a sequence of contracting rectangles is obtained, $\mathbf{R}_0$, $\mathbf{R}_1$, … with the properties that

$$\mathbf{R}_0 \supset \mathbf{R}_1 \supset \mathbf{R}_2 .... \supset \mathbf{R}_k .... \tag{4.4}$$

The limit of this sequence of rectangles can be defined to be $\mathbf{R}_\infty$. Since **E** is a subset of each $\mathbf{R}_k$, **E** is also a subset of $\mathbf{R}_\infty$. We can summarize the results of this development which constitutes the proof of the following theorem.

Theorem: If $\mathbf{R}_0$ is a rectangle that bounds all possible output voltages for a circuit with two feedback loop break points as constrained by the supply voltages and $<\mathbf{R}_k>$ is a contracting sequence of rectangles that satisfies the relationship $\boldsymbol{R}_{k+1} \subset f(\boldsymbol{R}_k)$ for all $k \geq 0$ with $\boldsymbol{R}_\infty = \lim_{k\to\infty} < \boldsymbol{R}_k >$, then if $\mathbf{R}_\infty$ is a point, the feedback circuit will have a single stable equilibrium point and this operating is $\mathbf{R}_\infty$.

Note that in the development of this theorem, the only restrictions that were placed on the bounding rectangles were that $\mathbf{A}_k \subset \mathbf{R}_{k+1}$ and $\mathbf{R}_{k+1} \subset \mathbf{R}_k$. If the rectangles that satisfy this relationship are too large, it may take a large number of steps to obtain convergence or the sequence may converge to a region, not to a single point, even if the circuit has a single stable equilibrium point. For example, each $\mathbf{R}_k$ could be simply $\mathbf{R}_0$ and this sequence of rectangles does not contract. So, it is often advantageous to define the rectangles in this sequence so that they are the smallest or nearly the smallest rectangles that includes $\mathbf{A}_k$. It should also be noted that this theorem states a sufficient but not a necessary condition for showing that a system has a single stable equilibrium point. For example, it is conjectured that there are circuits where even a set of minimum-sized rectangles will not converge to a single point even if the circuit contains a single stable equilibrium point. This algorithm could also be modified to identify multiple stable or even unstable equilibrium points. This modification would include provisions for separating $\mathbf{A}_k$ into disjoint regions, each of which contain an equilibrium point, and creating multiple sequences of bounding rectangles where

each sequence corresponds to a single equilibrium point. None of these issues, however, are germane to using this theorem to show that the circuit of Figure 4-5 has a single stable equilibrium point.

This algorithm and correspondingly this theorem will now be applied to the circuit of Figure 4-5.

i. Define the rectangle $\mathbf{R}_0$ to be $[0, V_{DD}]^2$. This serves as a bound for the output range for (V_o, V_{oP}).

ii. Perform a two-dimensional raster-scan input sweep over $\mathbf{R}_0$ to obtain $\mathbf{A}_0$=f($\mathbf{R}_0$).

iii. Bound the output datapoints ($\mathbf{A}_0$) by the minimum-sized rectangular boundary obtained from the finite set of data obtained with the raster-scan input sweep.

iv. Iterate the process until the sequence of rectangles converges to a very small rectangle which will define the resolution of the equilibrium point for the circuit.

Based on the test configuration as shown in Figure 4-6, the procedures to the two-dimensional raster-scan input sweep performed in Cadence Virtuoso are as follows:

1. Create two copies of the cascode temperature sensor circuit.
    a. On the first circuit, sweep V_i while making finite number of steps of V_{iP}.
    b. On the second circuit, sweep V_{iP} while making a finite number of steps of V_i.
    c. These sweeps are bounded by the rectangle $\mathbf{R}_k$ where $\mathbf{R}_0$ is $[0, V_{DD}]^2$.
2. Determine a rectangular boundary of the output voltages V_o and V_{oP} for the current iteration. Set the boundary maximum and minimum values to be the sweep range for V_i and V_{iP} on the next iteration, i.e. $\left[\min(V_o), \max(V_o)\right]_k \rightarrow \left[V_{iLo}, V_{iHi}\right]_{k+1}$ and

$V_{DD} - \left[\min\left(V_{oP}\right), \max\left(V_{oP}\right)\right]_k \rightarrow \left[V_{iPLo}, V_{iPHi}\right]_{k+1}$. The V_{DD} reference chosen for the sweeping voltage source V_{iP} is simply for convenience and the resulting output will be processed to maintain consistency with all points.

SIMULATION RESULTS

Simulation results for the circuit of Figure 4-6 will be presented here for five iterations. After five iterations, the bounding rectangle is quite small so this serves as a practical stopping point and allows us to draw the conclusion that the circuit has a single stable equilibrium point.

Simulation results for the first step in the iteration process are shown in Figure 4-7. In the left part of the figure, V_o vs V_i is shown for several different values of V_{iP}. From these results it can be seen that V_o is bounded below by 0.23V and bounded above by 0.749V. Note that this range on the output of 0.519V is considerably less than the range of 1.2V on the inputs V_i and V_{iP}. Thus in this first step in the iteration process a contraction in the output range of V_0 can be observed. The corresponding results for V_{iP} and V_{oP} are shown in the right part of the figure. Strictly for convenience, this simulation was run with V_{iP} referenced to V_{DD} and the simulation results for V_{oP} are presented with respect to V_{DD}-V_{iP} on the horizontal axis. For the (V_{DD}-V_{iP})/V_{oP} pair, the output range is constrained to the interval [0.460V, 1.125V], which corresponds to the V_{oP} interval of [0.075V, 0.74V]. Thus V_{oP} is bounded below by 0.075V and bounded above by 0.74V. This range of 0.665V is also considerably less than the range of 1.2V on the inputs V_i and V_{iP}. Thus in this first step in the iteration process, a contraction in the output range of V_{oP} can also be observed. The

rectangular region defined by $0.23V<V_i<0.749V$ and $0.075<V_{iP}<0.74V$ will serve as the input rectangle for the second step in the iteration process.

Run 0

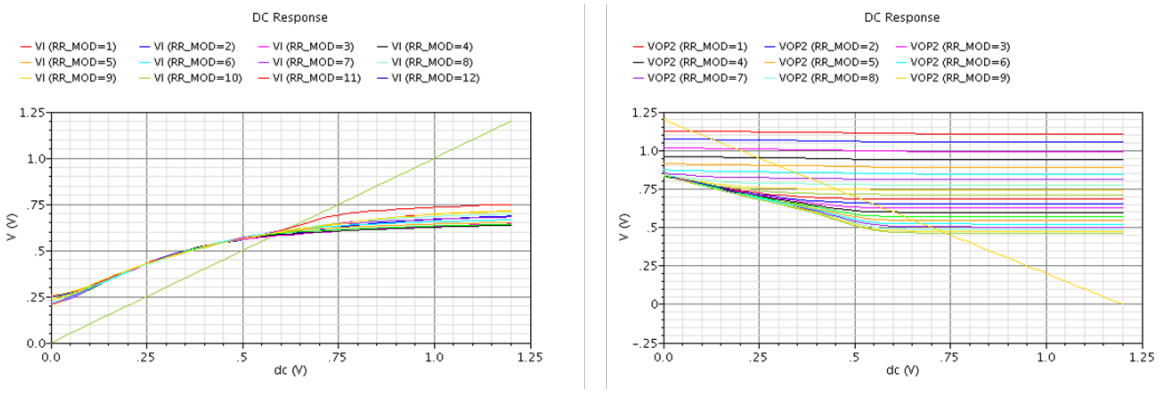


Figure 4-7: Run 0 simulation results, V_i/V_o (left) and $(V_{DD}-V_{iP})/V_{oP}$ (right)

Simulation results for the second step in the iteration process are shown in Figure 4-8. For the V_i/V_o pair, the V_o voltage is constrained to the interval [0.386V, 0.647V] and this will bound the Vi component of the rectangle for the third step in the iteration process. For the $(V_{DD}-V_{iP})/V_{oP}$ pair, the output range is constrained to the interval [0.613V, 0.940V] which corresponds to the V_{oP} interval of [0.260V, 0.587V]. This will bound the V_{oP} component of the rectangle for the third step in the iteration process. Thus additional contraction of the rectangle has occurred at the second step in the iteration process.

Run 1

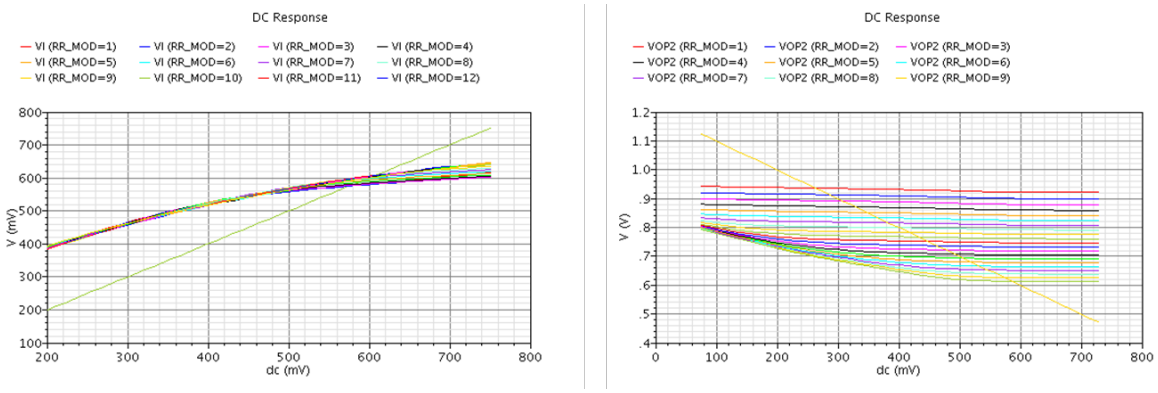


Figure 4-8: Run 1 simulation results, V_i/V_o (left) and $(V_{DD}-V_{iP})/V_{oP}$ (right)

Simulation results for the next four steps in the iteration process are shown in Figure 4-9, Figure 4-10, Figure 4-11, and Figure 4-12. The voltage V_o at each subsequent step in the iteration process has continued to contract with the output ranges being successively constrained by the intervals [0.509V, 0.620V], [0.567V, 0.612V], [0.590V, 0.609V], and [0.599V, 0.606V]. Correspondingly, the voltage V_{oP} at each subsequent step in the iteration process has continued to contract with the output ranges being successively constrained by the intervals [0.393V, 0.539V], [0.446V, 0.524V], [0.495V, 0.520V], and [0.508V, 0.518V].

Run 2

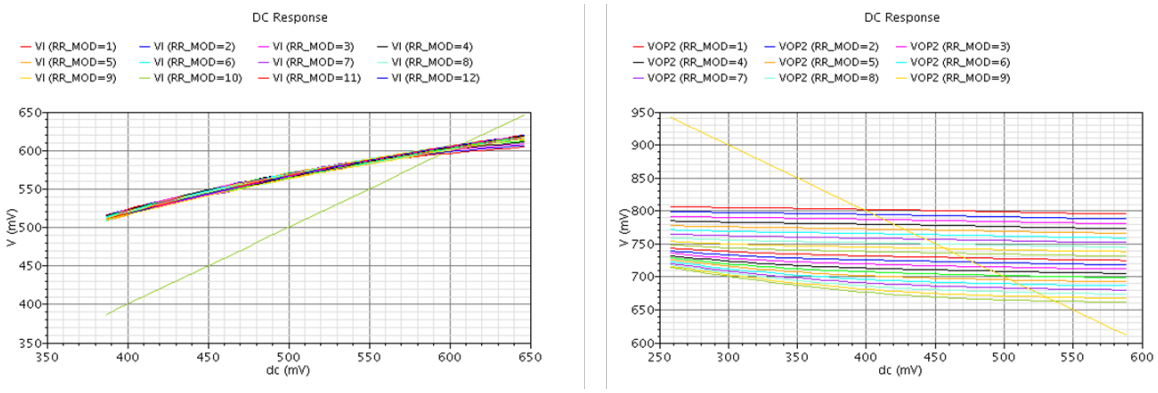


Figure 4-9: Run 2 simulation results, V_i/V_o (left) and $(V_{DD}-V_{iP})/V_{oP}$ (right)

Run 3

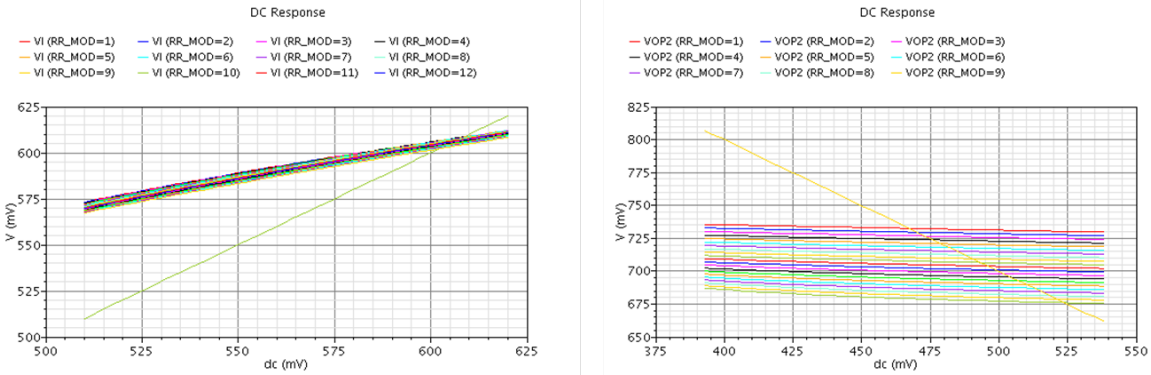


Figure 4-10: Run 3 simulation results, V_i/V_o (left) and $(V_{DD}-V_{iP})/V_{oP}$ (right)

Run 4

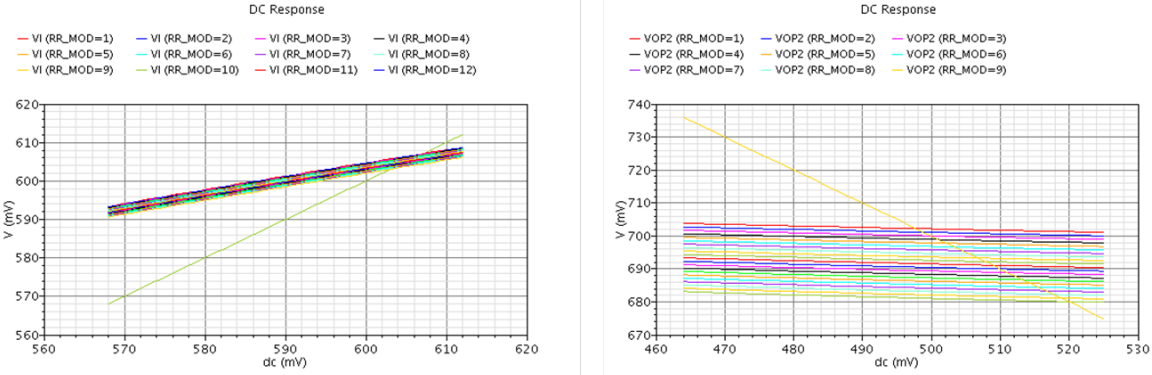


Figure 4-11: Run 4 simulation results, V_i/V_o (left) and $(V_{DD}-V_{iP})/V_{oP}$ (right)

Run 5

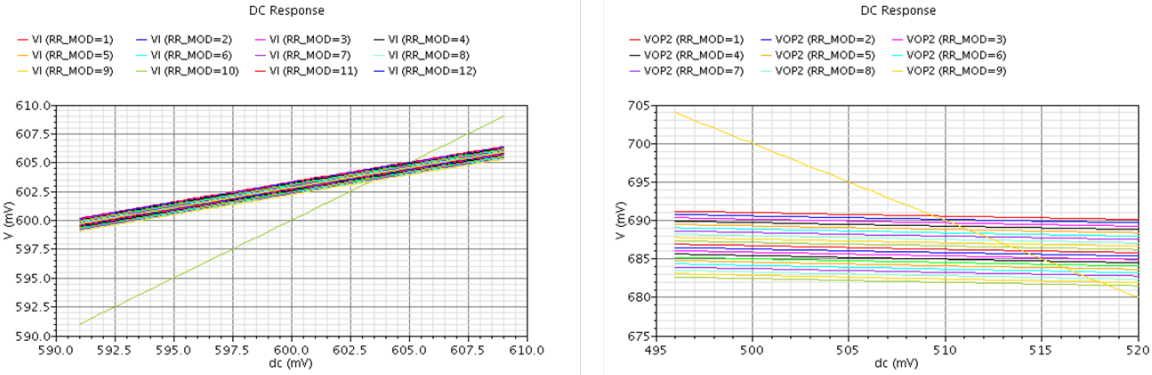


Figure 4-12: Run 5 simulation results, V_i/V_o (left) and $(V_{DD}-V_{iP})/V_{oP}$ (right)

The iteration process was stopped after Run 5. After these five steps, the rectangular region that bounds all equilibrium points is quite small. Though not shown in the simulations presented in this thesis, the boundaries on the rectangle will continue to contract and will approach a point in the limit as the number of iterations approaches infinity.

The regions corresponding to the outputs V_o and V_{oP} with the successive rectangular input regions are shown respectively in Figure 4-13 and Figure 4-14. Although the input was rectangular range at each step in the iteration, the region spanned by the output is far from rectangular for the output V_{oP}. Regardless, the contraction in the output regions which corresponds to the regions denoted by the $\mathbf{A}_k$'s above should be apparent from these plots.

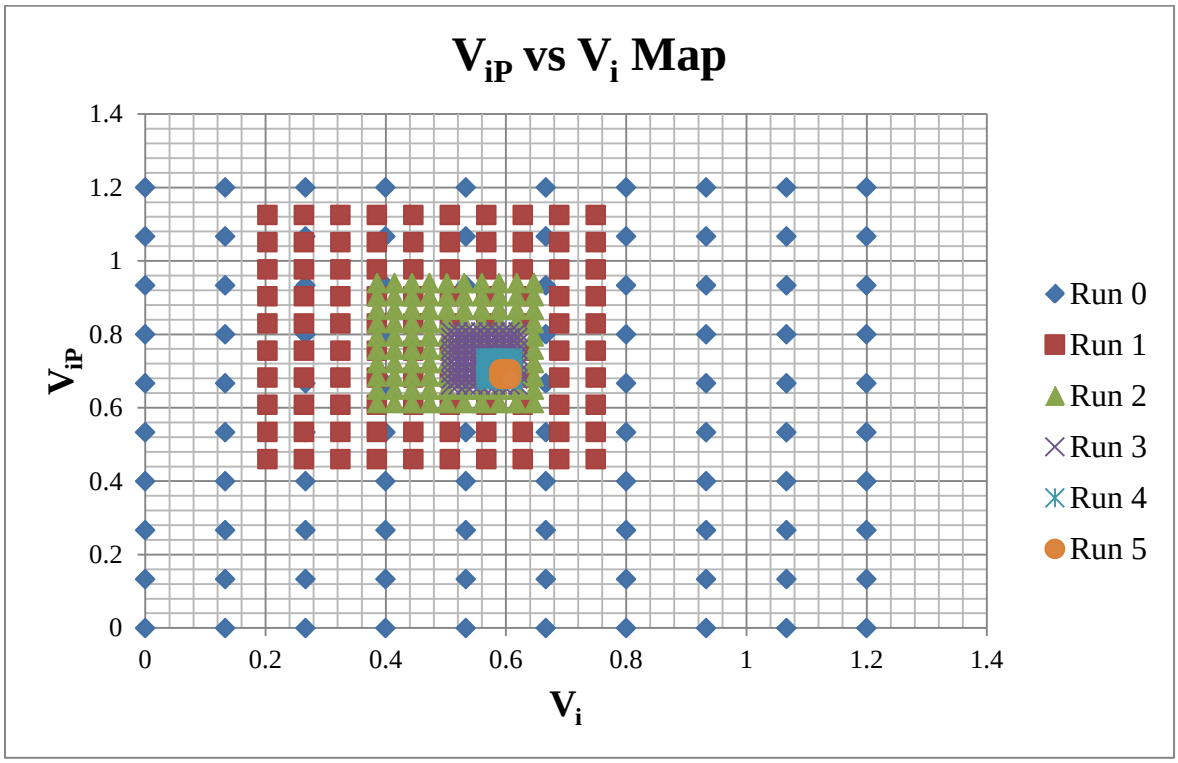


Figure 4-13: V_{iP} vs V_i Map for 6 iterations

Since the rectangular regions that bound the outputs are contracting and since they will continue to contract in the limit to a single point as the number of iterations go to infinity,

it can be concluded that the cascoded self-biased circuit has only one stable equilibrium point. Since there is a single stable equilibrium point, it follows that the circuit does not require a start-up circuit to guarantee proper operation.

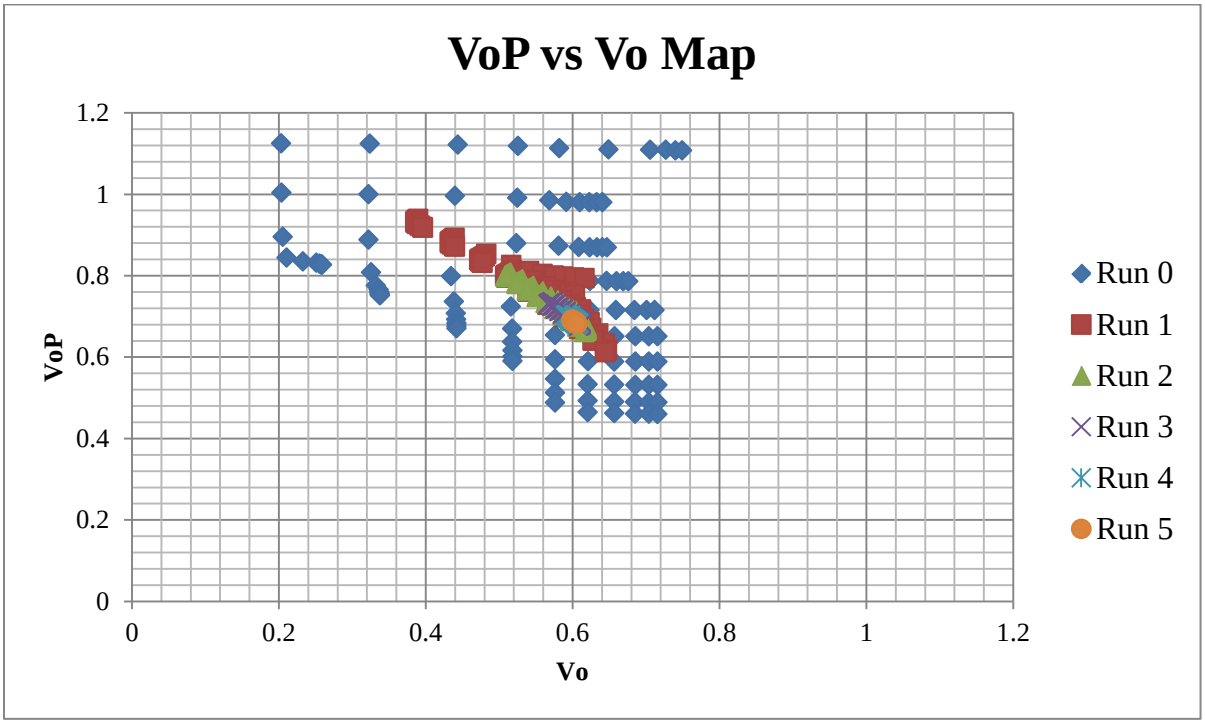


Figure 4-14: V_{oP} vs V_o Map for 6 iterations

In summary, a method has been introduced for identifying equilibrium points in a circuit that has more than one feedback loop. It is based upon an iterative contraction procedure that is suitable for computer simulation which provides sufficient but not necessary conditions for determining the equilibrium points in multiple feedback-loop circuits. This method has been used to show that the specific implementation of the cascode self-biasing temperature sensor introduced in this thesis has a single stable equilibrium point. It is conjectured that this iterative procedure will be useful for identifying the location of equilibrium points in other multiple feedback-loop circuits as well.

CHAPTER 5 CONCLUSIONS AND FUTURE WORK

This work focuses on the analysis and synthesis of a multiple-VT based threshold voltage extraction circuit for temperature sensing application. Built upon the fundamentals of Widlar and reverse Widlar CMOS reference generator circuit, the circuit senses temperature through the direct expression of the MOS threshold voltages, which are modeled to be linear with temperature [**19**]. While the reverse Widlar based temperature sensors are capable of achieving output voltages which are highly linear with respect to temperature, the relatively large voltage headroom requirement severely limits their performance and the effectiveness of cascoding under low supply voltages. Thus, the multi-VT transistors cell structure was proposed to address the voltage headroom issue and to significantly improve the V_{DD} sensitivity while providing good temperature sensing performance.

The basis of the multi-VT circuit is to exploit the natively available multiple threshold voltages devices in a digital deep submicron CMOS process. In comparison to the recent pn-junction based temperature sensors, it is found that the CMOS bipolar transistors' (BJT) effective gain is severely reduced (reaching unity) in deep submicron CMOS process [**30**]. As a result, CMOS BJT becomes less attractive and non-trivial to implement as the process feature size goes smaller. On the other hand, the proposed circuit utilizes only transistors operating in saturation region and its fundamental structure is simply 2-inverters in a loop. Hence, it is well suited for implementation in small feature size digital process with low supply voltage.

To demonstrate the claimed advantages of the proposed circuit, a multi-VT based cascode temperature sensor is implemented in 1.2V 65nm digital process. The temperature

sensor, through simulated results, is capable of sensing temperature in the range between -20˚C to 100 ˚C with maximum temperature INL of 0.351˚C at typical corner. At the nominal temperature coefficient of -0.944mV/˚C, the maximum temperature error due to ±10% supply variation is only 0.44˚C. Let the total temperature error to be the sum of absolute maximum temperature INL and temperature error due to ±10% supply variation. Then, the total temperature error affecting the proposed circuit under typical condition is 0.791˚C (less than 1˚C). The maximum RMS temperature error due to noise over a period of 10 years is found to be 0.38˚C.

A unique feature of this work is showing that the proposed circuit has only 1 stable equilibrium point. Viewing the 4-transistors basis cell as 2 inverters in a loop and evaluating its DC transfer characteristics allow clear interpretation if the circuit has multiple stable equilibrium points. The results for the multi-VT 4-transistors cell indicate that it has only 1 stable equilibrium point and does not require a startup circuit. This is a big advantage because eliminating the startup circuit can save more area and potentially reduce the overall power consumption. When the multi-VT circuit is cascoded, self-biasing scheme is used to bias the cascode transistors, introducing extra loops and risks of the circuit having multiple stable equilibrium points. Using the iterative process similar to the idea of the Contraction Mapping Principle, the transfer characteristics of the cascode circuit were obtained. The results show that the specific implementation of the cascode circuit introduced in this thesis has a single stable equilibrium point and hence it does not require a startup circuit.

The multi-VT circuit structure is recognized to have potential to serve as reference generators in low-voltage deep-submicron digital process. The exploitation of multiple

threshold devices can be further expanded to realize new classes of analog circuits. As for the proposed temperature sensor design, more effort can be put to optimize the key performance parameters using the analysis done in this work. An efficient scheme for temperature-to-digital conversion can be implemented with the proposed circuit as the analog front-end to create a smart temperature sensor.

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Sincerely,

Alex Sheng-Huang Lee

BIBLIOGRAPHY

[1] Neil H. E. Weste and David Money Harris, *CMOS VLSI Design A Circuits and Systems Perspective*, 4th ed. USA: Addison Wesley, 2010.

[2] ITRS. (2010) ITRS 2010 Update. [Online]. http://www.itrs.net/Links/2010ITRS/Home2010.htm

[3] Intel Corporation. (2011, April) Performance + Reliability + Security = Intel Xeon Processor Formula for Mission-Critical Computing. [Online]. http://newsroom.intel.com/community/intel_newsroom/blog/2011/04/05/performance-reliability-security-intel-xeon-processor-formula-for-mission-critical-computing

[4] NVIDIA Corporation. (2011, April) GeForce GTX 590. [Online]. http://www.geforce.com/#/Hardware/GPUs/geforce-gtx-590/specifications

[5] Intel Corporation. (2007, June) Mobile Intel 965 Express Chipset Family Datasheet, Revision 3.

[6] Advanced Micro Devices Inc. (2004, June) AMD Functional Data Sheet, 940 Pin Package Rev 3.05.

[7] James R. Black, "Electromigration Failure Modes in Aluminum Metallization for Semiconductor Devices," *Proceedings of the IEEE*, vol. 57, no. 9, pp. 1587-1594, September 1969.

[8] Philip E. Allen and Douglas R. Holberg, *CMOS Analog Circuit Design*, 2nd ed. USA: Oxford University Press, 2002.

[9] E. Vittoz and J. Fellrath, "CMOS analog circuits based on weak inversion operation," *Solid-State Circuits, IEEE Journal of*, vol. 12, no. 3, pp. 224-231, June 1977.

[10] R. Jacob Baker, *CMOS Circuit Design, Layout, and Simulation*, 3rd ed.: Wiley-IEEE Press, 2010.

[11] R. Wassenaar. (1996, October) Analysis of Analog C-MOS Circuits. Ph.D. Dissertation, Twente University, The Netherlands.

[12] Behzad Razavi, *Design of Analog CMOS Integrated Circuits*.: McGraw Hill, 2001.

[13] G. Matramga, L. Coco, and G. Compagno, "CMOS Temperature Sensor," US Patent 6,489,831, December 3, 2002.

[14] H.J. Oguey and D. Aebuscher, "CMOS current reference without resistance," *Solid-State Circuits, IEEE Journal of*, vol. 32, no. 7, pp. 1132-1135, July 1997.

[15] Y. Moon and D. Jeong, "Voltage-Controlled Osccillator Resistant to Supply Voltage Variation," US Patent 5,955,929, September 21, 1999.

[16] V. Székely, M. Rencz, S. Török, Cs. Márta, and L. Lipták-Fegó, "CMOS temperature sensors and built-in test circuitry for thermal testing of ICs," *Sensors and Actuators A: Physical*, vol. 71, no. 1-2, pp. 10-18, November 1998.

[17] Jun He, Chen Zhao, Sheng-Huang Lee, and Karl Peterson, "A linear very compact untrimmed on chuo temperature sensor with second and third order temperature compensation," in *Circuits and Systems (MWSCAS), 2010 53rd IEEE International Midwest Symposium on*, Seattle, 2010, pp. 288-291.

[18] Jun He. (2010) Analyses and design strategies for fundamental enabling building blocks: Dynamic comparators, voltage references and on-die temperature sensors. Ph.D. Dissertation Iowa State University.

[19] Tanvir Hasan Morshed et al. (2009) BSIM4.6.4 MOSFET Model - User's Manual. Department of Electrical Engineering and Computer Sciences, University of California, Berkeley.

[20] STMicroelectronics. (2006, June) How to achieve the threshold voltage thermal coefficient of the MOSFET acting on design parameters. AN2386 Application note.

[21] Paul R. Gray, Paul J. Hurst, Stephen H. Lewis, and Robert G. Meyer, *Analysis and Design of Analog Integrated Circuits*, 5th ed. USA: Wiley, 2009.

[22] G.C.M. Meijer, "Thermal sensors based on transistors," *Sensors and Actuators*, vol. 10, pp. 103-125, 1986.

[23] M Sasaki, M Ikeda, and K Asada, "A temperature sensor with an inaccuracy of -1/0.8°C using 90-nm 1-V CMOS for online thermal monitoring of VLSI circuits," *Semiconductor Manufacturing, IEEE Transactions on*, vol. 21, no. 2, pp. 201-208, May

2008.

[24] Poki Chen, Chun-Chi Chen, Chin-Chung Tsai, and Wen-Fu Lu, "A time-to-digital-converter-based CMOS smart temperature sensor," *Solid-State Circuits, IEEE Journal of*, vol. 40, no. 8, pp. 1642-1648, August 2005.

[25] J. Georgiou and C. Toumazou, "A resistorless low current reference circuit for implantable devices," in *Ciruits and Systems, 2002 (ISCAS). IEEE International Symposium on*, 2002, pp. III-193 - III-196.

[26] Takeshi Shima, "Temperature insensitive current reference circuit using standard CMOS devices," in *Circuits and Systems, 2007 (MWSCAS). 50th Midwest Symposium on*, 2007, pp. 181-184.

[27] Nor Hisham Hamid, Alan F. Murray, and Scott Roy, "Time-Domain Modeling of Low-Frequency Noise in Deep-Submicrometer MOSFET," *IEEE Transactions on Circuits and Systems - I: Regular Papers*, vol. 55, no. 1, pp. 245-257, February 2008.

[28] H. Sanchezm and et al., "Thermal Management Systems for High Performance PowerPC Microprocessors," in *IEEE Compcon*, 1997, pp. 325-330.

[29] M. Pertijs, K. Makinwa, and J. Huijsing, "A CMOS Smart Temperature Sensor with a 3σ Inaccuracy of ±1°C from -55°C to 125°C," *IEEE Journal of Solid State Circuits*, vol. 40, pp. 2805-2815, December 2005.

[30] Fabio Sebastiano et al., "A 1.2-V 10-μW NPN-Based Temperature Sensor in 65-nm

CMOS with an Inaccuracy of 0.2°C (3σ) From -70°C to 125°C," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 12, pp. 2591-2601, December 2010.

[31] Hasnain Lakdawala, Y. William Li, Arijit Raychowdhury, Greg Taylor, and Krishnamurthy Soumyanath, "A 1.05V 1.6mW, 0.45°C 3σ Resolution ΔΣ Based Temperature Sensor With Parasitic Resistance Compensation in 32nm Digital CMOS Process," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 12, pp. 3621-3630, December 2009.

[32] B. Datta and W. Burleson, "Low-power and robust on-chip thermal sensing using differential ring oscillators," in *IEEE Midwest Symposium on Circuits and Systems*, 2007, pp. 29-32.

[33] K. Kim, H. Lee, S. Jung, and C. Kim, "366kS/s 400uW 0.0013mm2 Frequency-to-Digital Converter Based CMOS Temperature Sensor Utilizing Multiphase Clock," in *IEEE Custom Integrated Circuits Conference*, 2009, pp. 203-206.

[34] Krzysztof Ciesielski, "On Stefan Banach and Some of His Results," *Banach Journal of Mathematical Analysis*, vol. 1, pp. 1-10, 2007.

[35] Keith Conrad. The Contraction Mapping Theorem. [Online]. www.math.uconn.edu/~kconrad/blurbs/analysis/contractionshort.pdf